

Experiment 2

Diode-Resistor Logic (DRL) Gates

Objectives:

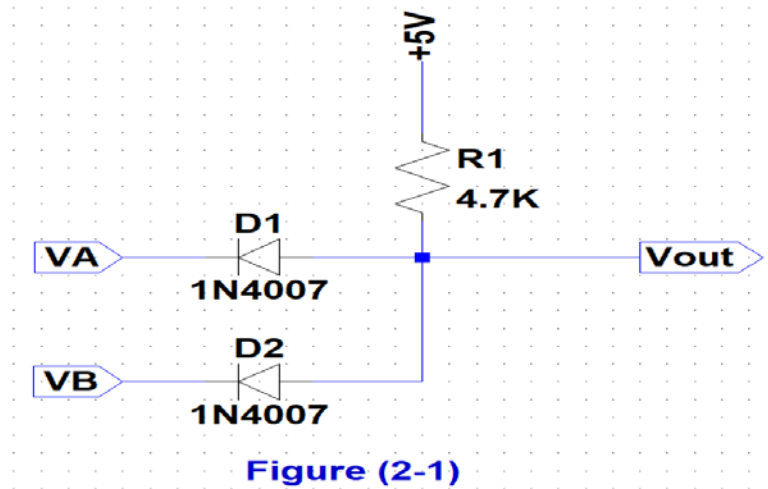
- To be familiar with the operation of diode-resistor logic circuits.
- To determine VTC of these gates.

Theoretical Background:

1. Diode-resistor logic (DRL):

The diode-resistor logic circuits consist of diodes and resistor only, the logic functions available are AND, OR, level-shifted AND and level-shifted OR.

• AND Gate:



For the diode-resistor AND gate, figure (2-1), the output voltage can be represented the truth table, "1 for input high, 0 for input low".

VA	VB	VOUT
0	0	0
1	0	0
0	1	0
1	1	1

- If any of the input is low, the corresponding diode is allowed to conduct, and $V_O = V_D + V_{in}$
- If the two inputs are high, the diodes are off and $V_O = V_{cc}$.

- **OR Gate:**

For the diode-resistor OR gate, fig.(2-2), the output voltage can be represented by the truth table,” 1 for input high, 0 for input low”.

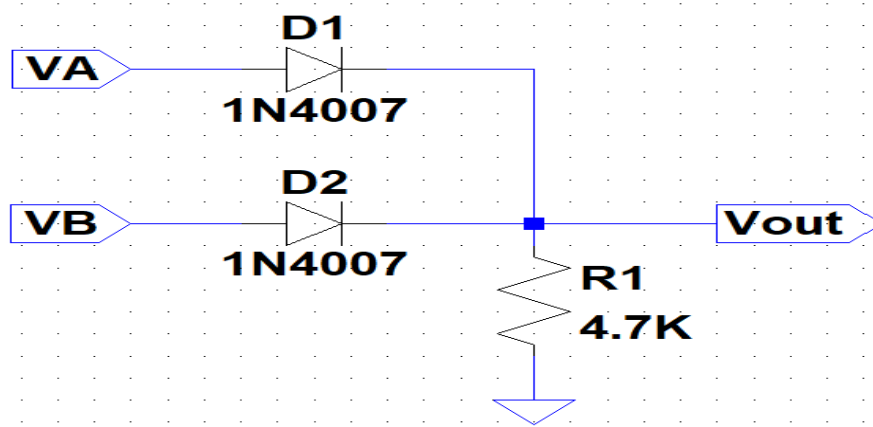


Figure (2-2)

VA	VB	VOUT
0	0	0
1	0	1
0	1	1
1	1	1

Fig(2-2) shows a DRL circuit, which provides the function of a 2-inputs OR gate. It is possible to add any number of input diodes to this circuit, each with its separate input signal. If any input is set to logic 1 (+5 V), the corresponding diode will conduct and the VOUT will be equal to (5 V- 0.7 V = 4.3 V), which stands for logic 1. When both inputs are set to logic 0 (grounded), both diodes will be reverse biased (cutoff) and VOUT will be equal to 0 (logic 0).

- **Level-Shifted AND Gate:**

A level Shifting diode D has been added to the diode-resistor AND gate as in fig.(2-3).

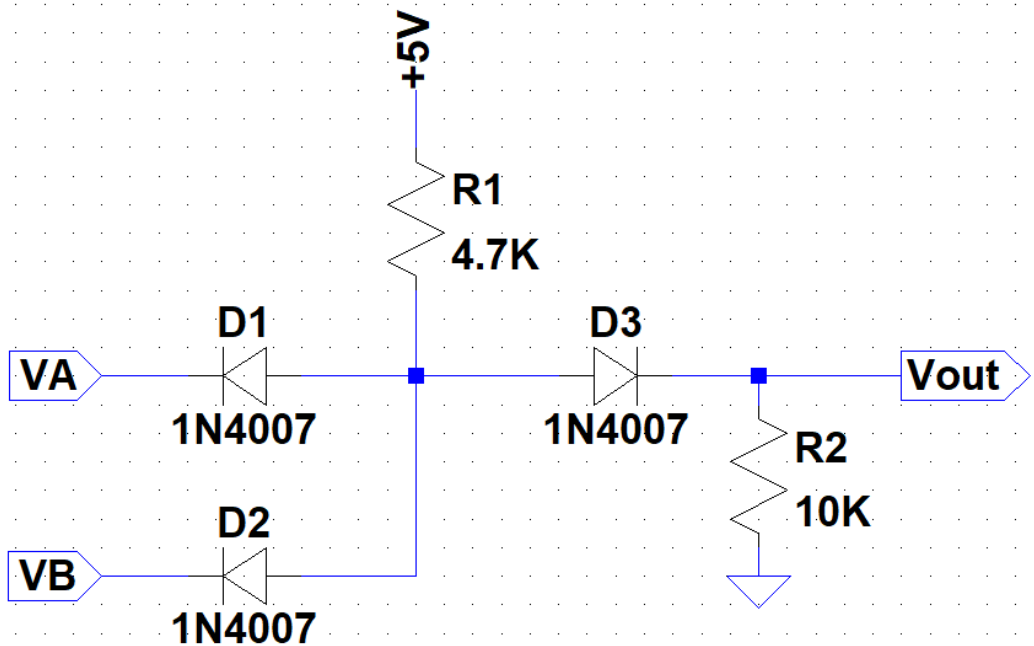


Figure (2-3)

- If any input is low, its corresponding diode is conducting, and the output voltage $V_o = V_{in} + V_{D1} - V_{D3} = V_{in}$.
- If $V_{in} (V_A, V_B) < -V_{ee}$, the diodes D1, D2 are off, and the output voltage $V_o = -V_{ee} = V_{ol}$.
- For all inputs are high (greater than $V_{dc} - V_{D1} = V_{dc} - V_{D2}$)
 $V_o = V_{oh}$
 $I_D = (V_{cc} + V_{ee} - V_{D3}) / (R_1 + R_2)$
 $V_{oh} = -V_{ee} + I_D \cdot R_2$

- **Level-Shifted OR Gate:**

Level shifting diode D has been added to the diode-resistor OR gate as in fig.(2-4).

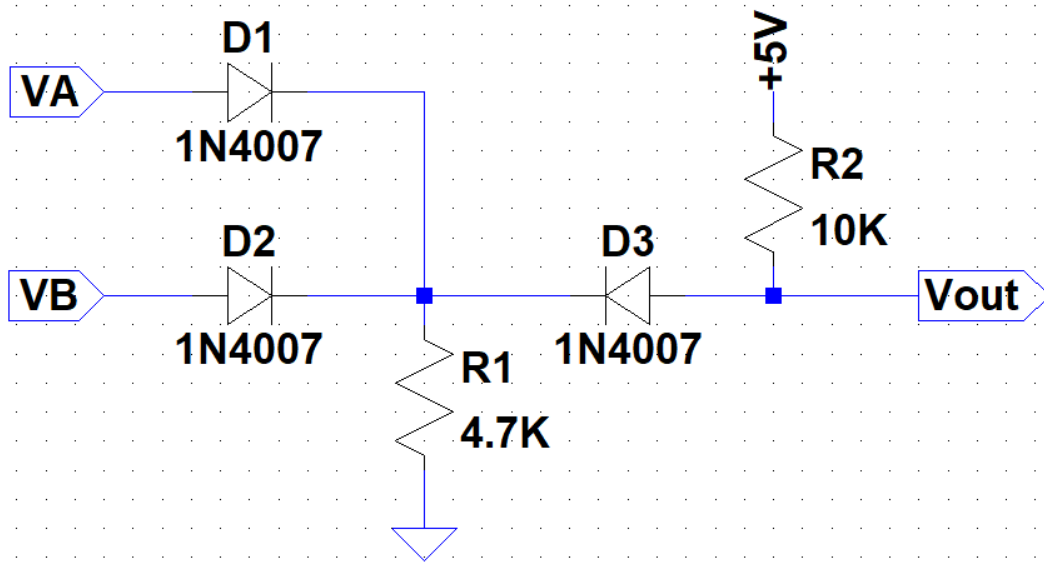


Figure (2-4)

- If all inputs are low, the diodes off,

$$I_D = (V_{CC} + V_{EE} - V_{D3}) / (R_1 + R_2)$$

$$V_{OL} = V_{CC} - I_D \cdot R_2$$
- If either input is high, the corresponding diode is conducting then

$$V_O = V_{OH} = V_{in} - V_{D2} + V_{D3} = V_{in}.$$

Experimental Procedure & Report tasks:

Note: Write your name and ID on each screenshot.

Part (1): AND Gate Truth table:

- 1) Connect the AND gate circuit shown in Fig. (2-1) using LTSpice.
- 2) Investigate its truth table by using Transient Analyses as follows:
 - **VA:** Pulse wave with $V_{initial}=0V$, $V_{on}=5V$, $T_{delay}=0SEC$, $T_{rise}=0.0001SEC$, $T_{fall}=0.0001SEC$, $T_{on}=1SEC$, $Period=2SEC$, $N_{cycles}=1$.
 - **VB:** Pulse wave with $V_{initial}=0V$, $V_{on}=5V$, $T_{delay}=0SEC$, $T_{rise}=0.0001SEC$, $T_{fall}=0.0001SEC$, $T_{on}=0.5SEC$, $Period=1SEC$, $N_{cycles}=2$.

Attach screenshot showing the circuit and the results.

Part (2): OR Gate Truth table:

- 1) Connect the OR gate circuit shown in Fig. (2-2) using LTSpice.
- 2) Investigate its truth table by using Transient Analyses as follows:
 - **VA:** Pulse wave with $V_{initial}(V)=0$, $V_{on}(V)=5$, $T_{delay}(SEC)=0$, $T_{rise}(SEC)=0.0001$, $T_{fall}(SEC)=0.0001$, $T_{on}(SEC)=1$, $Period(SEC)=2$, $N_{cycles}=1$.
 - **VB:** Pulse wave with $V_{initial}(V)=0$, $V_{on}(V)=5$, $T_{delay}(SEC)=0$, $T_{rise}(SEC)=0.0001$, $T_{fall}(SEC)=0.0001$, $T_{on}(SEC)=0.5$, $Period(SEC)=1$, $N_{cycles}=2$.

Attach screenshot showing the circuit and the results.

Part (3): Level-Shifted AND Gate VTC:

- 1) Connect the level-shifted AND gate circuit shown in Fig. (2-3) using LTSpice.
- 2) Connect the inputs VA and VB to the same Voltage Source.
- 3) Plot the voltage transfer characteristics (VTC) of the level shifted AND gate. Then determine V_{oh} & V_{ol} .

Vol	
Voh	

Note: let V_{in} increases from -2V to 5V.

Part (4): Level-Shifted OR Gate VTC:

- 1) Connect the level-shifted OR gate circuit shown in Fig. (2-4) using LTSpice.
- 2) Connect the inputs VA and VB to the same Voltage Source.
- 3) Plot the voltage transfer characteristics (VTC) of the level shifted AND gate.
Then determine Voh & Vol.

Vol	
Voh	

Note: let Vin increases from 0V to 7V.