

Experiment 3

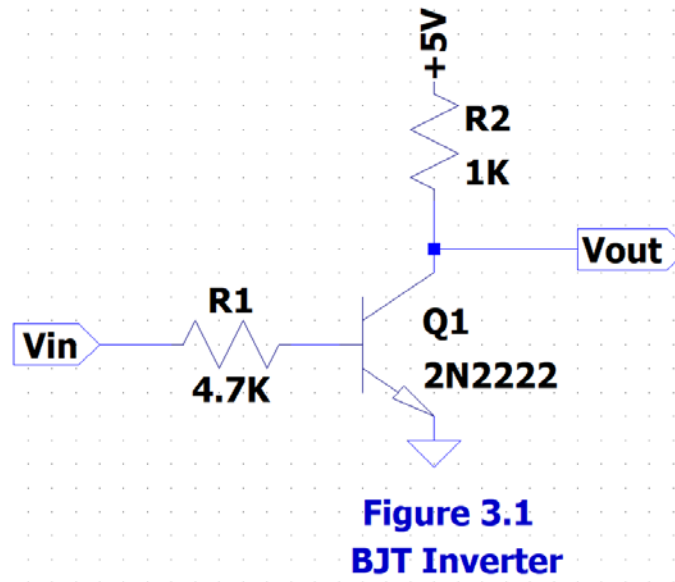
Resistor-Transistor Logic (RTL) Gates

Objectives:

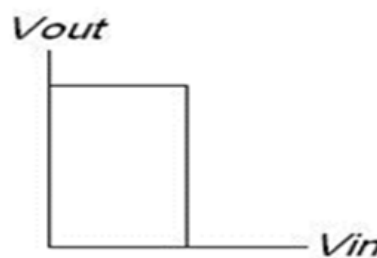
- To be familiar with the operation of BJT Inverter.
- Be familiar with logic gates using resistors and bipolar transistor connected with RLT techniques.
- Studying the internal connection of AND, OR, NAND, and NOR.
- To determine the VTC of these gates.

Theoretical Background:

1. Inverter Gate



The ideal Inverter model is important because it gives a metric by which we can judge the quality of actual implementation. Its VTC is shown in figure 3.2 and has the following properties: Infinite gain in the transition region, and gate threshold located in the middle of the logic swing, with high and low margins equal to the half of the swing. The input and output impedance of the ideal gate are infinity and zero, respectively.



Dynamic Behavior of Inverter Digital Gate:

Figure 3.3 illustrates the behavior of the inverter digital gate using BJT

There are three regions for the voltage transfer characteristic:

1. Cut-off region
2. Forward Active region
3. Saturation region

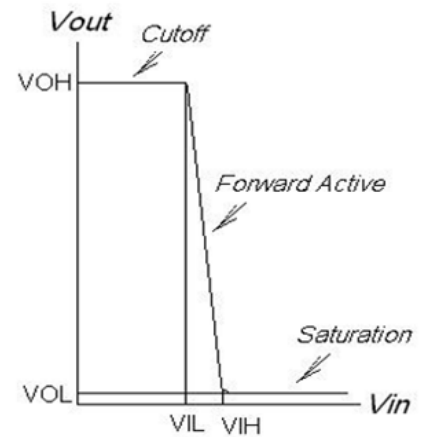


Figure 3.3

BJT Inverter can be best expressed by its voltage transfer characteristic (**VTC**) or DC transfer characteristic as shown in figure 3.3 That relates the output voltage to the input one.

If:

- $V_i = V_{ol}$, $V_o = V_{oh} = V_{cc}$ (VTC) or DC Transfer Characteristic The transistor is OFF.
- $V_i = \mathbf{V_{il}}$
The transistor Begins to turn on.
- $\mathbf{V_{il}} < V_i < \mathbf{V_{ih}}$
The transistor is in forward active region and operates as Amplifier.
- $V_i = V_{oh}$
The transistor will be deep is saturation, $V_o = V_{ce(sat)}$.

Noise:

Variations in voltage levels in digital circuits can cause logic errors, referred to as noise.

- ❖ A measure of sensitivity to noise is called **Noise Margin (NM)** which can be expressed by:

$$N_{ml} = V_{il} - V_{ol}$$

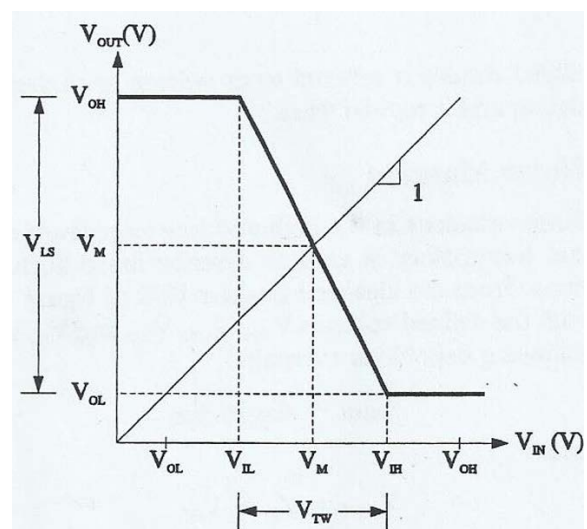
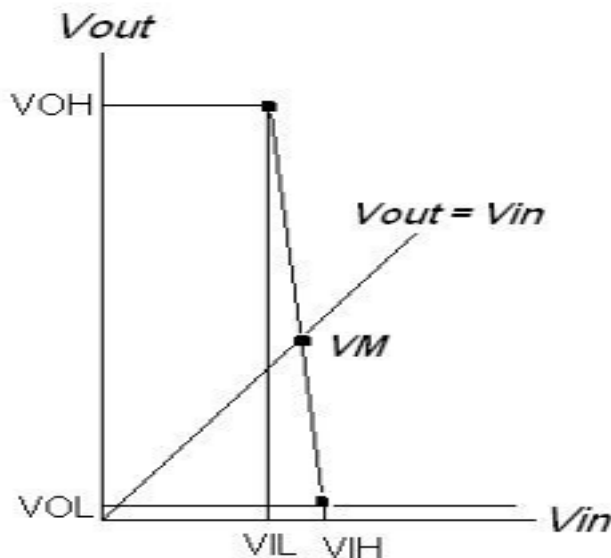
$$N_{mh} = V_{oh} - V_{ih}$$

The voltage noise margins represent a safety margin for the high and low voltage levels. Extraneous noise voltages must have magnitudes less than the voltage noise margins. The exact magnitudes of the high and low voltage level are not important. However, the high or low magnitude of voltage must remain in the range of voltages that provide **positive noise margins**.

- ❖ **Logic Swing:** $LS = V_{oh} - V_{ol}$

- ❖ We can calculate **The transition width** using the following expression $TW = V_{ih} - V_{il}$.

- ❖ **Midpoint Voltage V_M :** the point on the VTC at which $v_{in} = v_{out}$.



Transient Characteristics:

Digital logic circuits have finite switching speeds. That is, switching a voltage from high to low (or vice-versa) requires a finite amount of time. Additionally, when the input voltage changes from one level to another, the output voltage response is delayed in time. This is referred to as propagation delay. These limitations are present for all circuits and in particular digital logic circuits. For digital circuits employing BJTS, these time limitations are caused by the time required to store and remove charge from the base region. Section 4.5 discusses methods for decreasing the storage and removal times required by the base.

T_d : delay time

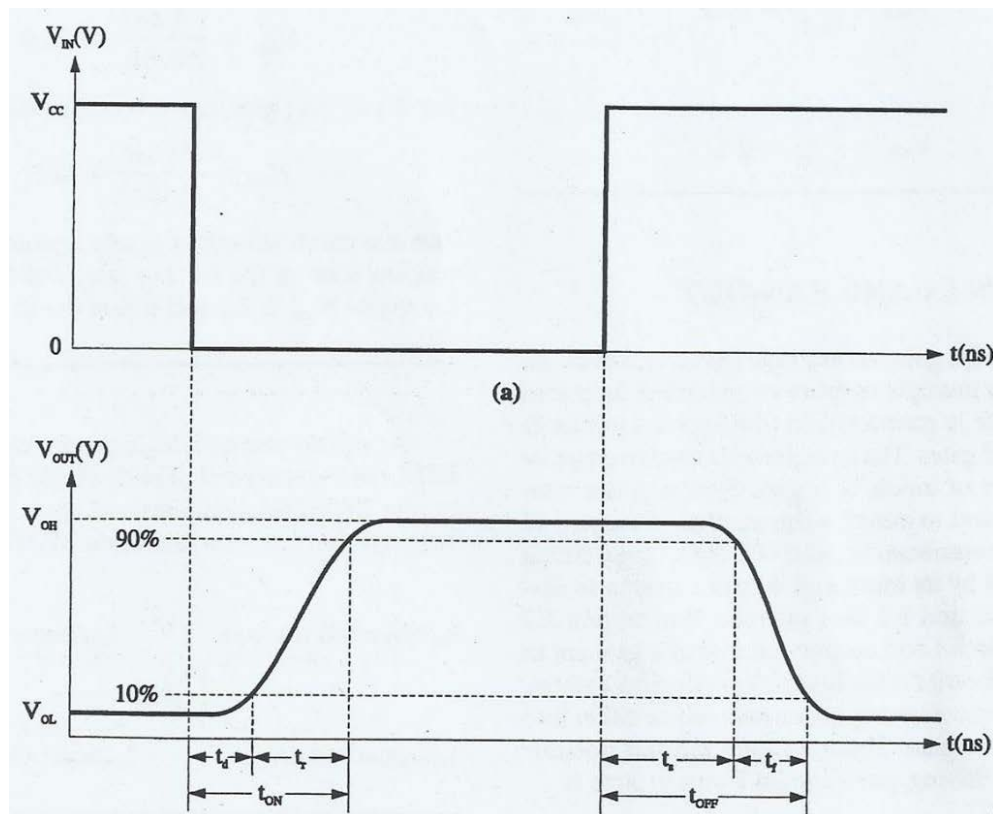
T_r : rising time

T_s : storage time

T_f : falling time

T_{on} : turn-on time = $T_d + T_r$

T_{off} : turn-off time = $T_s + T_f$



2-Input NOR gate

NOR gates are commonly used in integrated circuits because of the simple circuits that implement their function. Other types of gates can be built using combination of NOR gates, the NOR is a (functionally complete set).

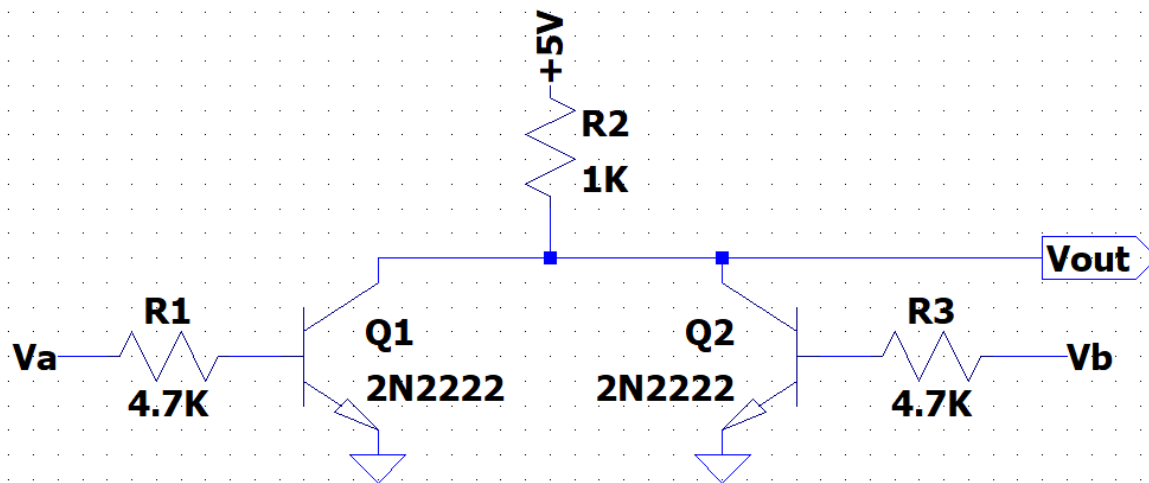


Figure 3.4
NOR Gate

For this circuit, the current through the single collector resistor is the sum of the BJT's and is given by

$$I_c = \sum I_{cI}$$

The output voltage is then

$$V_{out} = V_{cc} - I_c R_2$$

If all inputs are less than $V_{BE(FA)}$ then all BJT's are cutoff. As a result, $I_c=0$ and the output voltage is

$$V_{OH} = V_{cc}$$

If any input is greater than or equal to $V_{BE(FA)}$, the corresponding BJT conducts and if any input reaches V_p the output drops to

$$V_{OL} = V_{CE(SAT)}$$

2. 2-Input NAND gate

A very common NAND logic is the RTL series. The main advantage of such system is the Pull-down network.

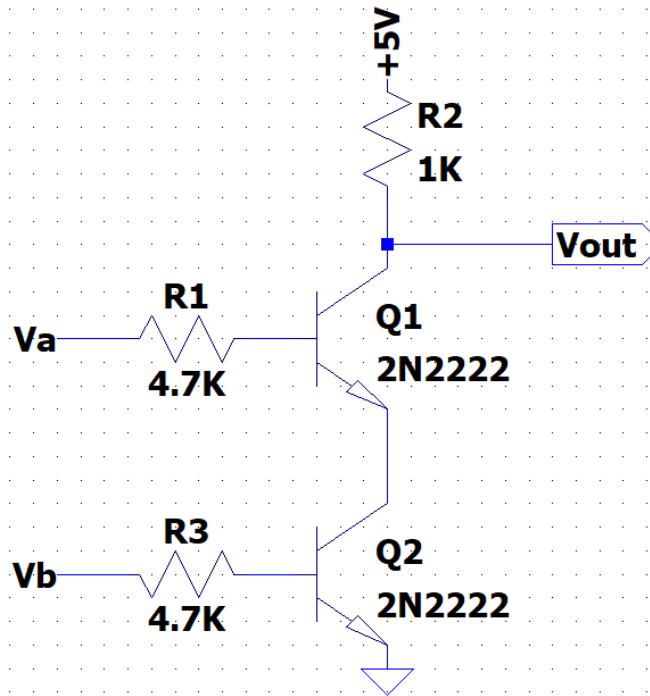


Figure 3.5
NAND Gate

If all inputs are greater than or equal V_{BE} (FA) then all BJTs conduct and the output voltage is

$$V_{Out} = V_{cc} - I_c R_2$$

If any input is low, the corresponding transistor is cutoff, and the output voltage is

$$V_{OH} = V_{cc}$$

If all inputs reach V_{IH} the output is

$$V_{OL} = 2 \times V_{CE(SAT)}$$

Experimental Procedure & Report tasks:

Note: don't forget to write your comments on each part

Part 1: Inverter Gate:

- 1- Connect the circuit shown in Figure 3.1 in LTspice.
- 2- Use DC-sweep analyses and sketch VTC, **attach the result**.
- 3- From the **result** and using the **calculations**, find:

Vil		TW	
Vih		LS	
Vol		Nml	
Voh		Nmh	

Part 2: 2-Input NOR gate:

1. Construct the circuit shown in Figure 3.4 in LTspice.
2. Investigate its truth table by using Transient Analyses using the method we learned in Lab 2.

Part 3: 2-Input NAND gate:

- 1) Connect the circuit shown in Fig. 3.5 using LTSpice.
- 2) Connect the inputs VA and VB to the same Voltage Source.
- 3) Plot the voltage transfer characteristics (VTC). Then determine Voh & Vol.

Vol	
Voh	

Note: let Vin increases from 0V to 2V.