

Experiment 4

Diode-Transistor Logic (DTL) Gates

Objectives:

- Be familiar with the diode-transistor logic DTL circuit.
- Studying the internal connection of AND, OR, NAND, and NOR.
- To determine the VTC of these gates.
- To find the advantages of this family over the RTL family.

Introduction

Circuits of the DTL family utilize diodes and BJTs in their design. As the name implies, the DTL family was introduced to improve the switching speed over the circuits of the RTL family. In 1964, a version of DTL was introduced and become the Standard digital IC family for nearly ten years.

In this experiment five circuits are introduced, the basic inverter, AND, OR, NAND, and NOR.

Theoretical Background:

❖ The basic DTL inverter

Figure 3-1 shows the DTL inverter, which could be built by replacing the resistor connected to the base of the transistor in the RTL inverter by a diode. This allows faster switching action. As a result, gates built with diodes in place of most resistors can operate at higher frequencies. Because of this Diode- Transistor logic, DTL Rapidly replaced RTL in most digital applications.

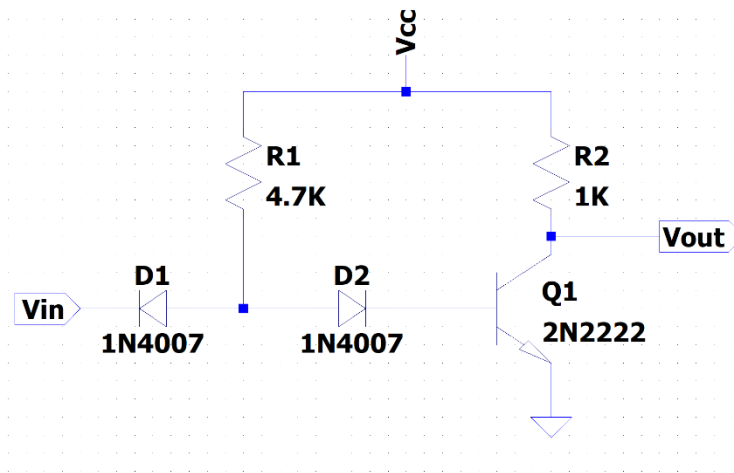


Figure 3-1
DTL Inverter

If the input is less than $V_{IL} = V_{BE}$ (FA) then the BJT is cutoff. As a result, the output voltage is

$$V_{OH} = V_{CC}$$

If the input is greater than or equal to V_{BE} (FA), the corresponding BJT conduct and if any input reaches $V_{IH} = V_{BE}$ (SAT) the output drops to

$$V_{OL} = V_{CE} \text{ (SAT)}$$

❖ The NAND gate

The DTL NAND gate combines the DTL inverter with simple DL AND gate. Signal Degradation caused by DL is overcome by the transistor, which amplifies the signal while inverting it. **Figure 3-2** shows a two-input NAND gate.

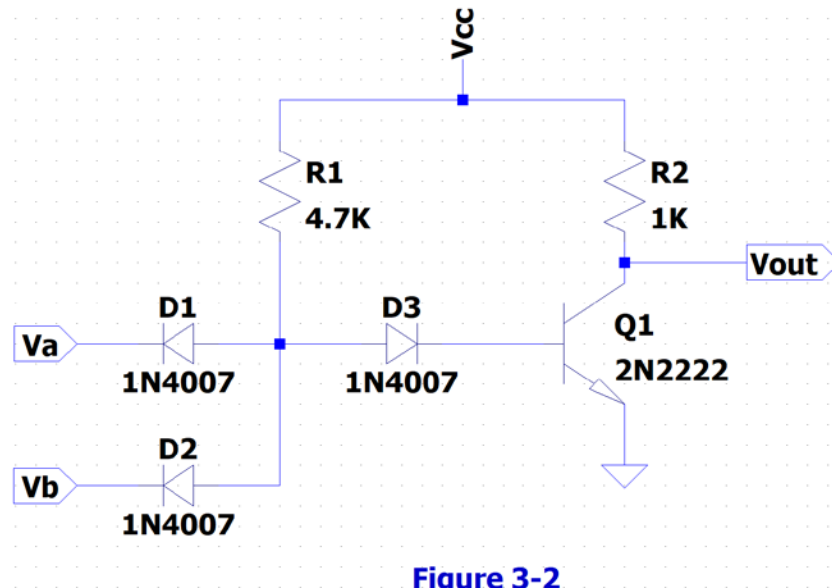


Figure 3-2

Two-input NAND Gate

If any input is less than $V_{IL} = V_{BE}$ (FA), the transistor is cut off and the output is $V_{OH} = V_{CC}$

if all inputs are greater than or equal to V_{BE} (FA), the BJT conducts and if they reach $V_{IH} = V_{BE}$ (SAT) the output is

$$V_{OL} = V_{CE} \text{ (SAT)}$$

❖ The AND gate

The DTL AND gate combines the DTL NAND gate and DTL inverter, **Figure 3** shows a two-input AND gate.

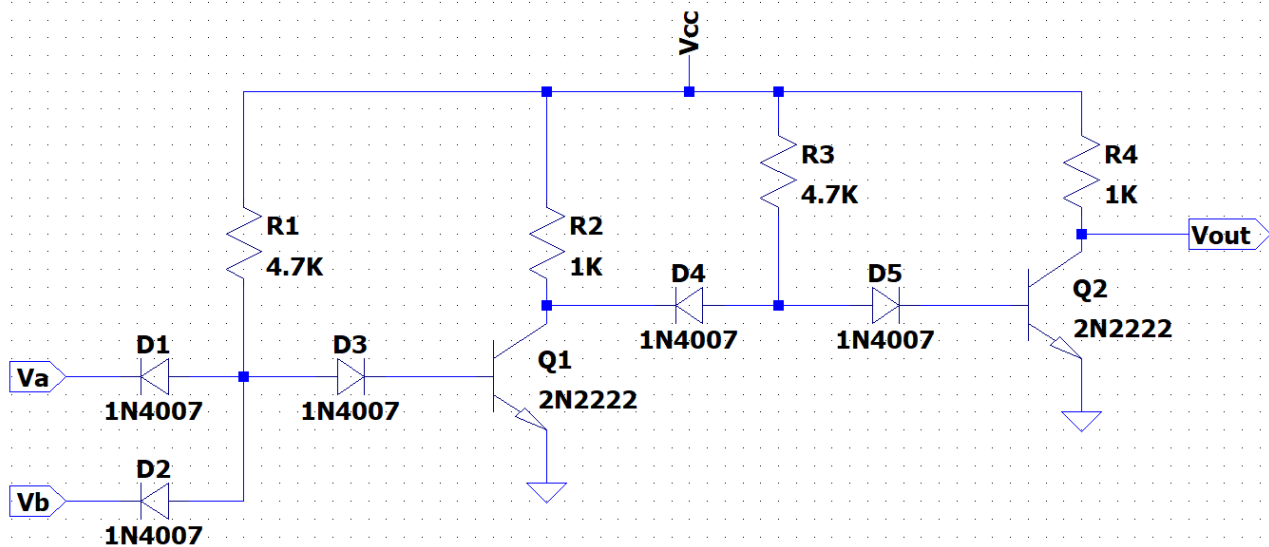


Figure 3-3

Two-input AND Gate

❖ The NOR gate

The DTL NOR gate combines multiple DTL inverters with a common output as shown in Figure 4. This is exactly the same as the method used to combine RTL inverters to form a NOR gate. Any number of inverters may be combined in this fashion to allow the required number of inputs to the NOR gate.

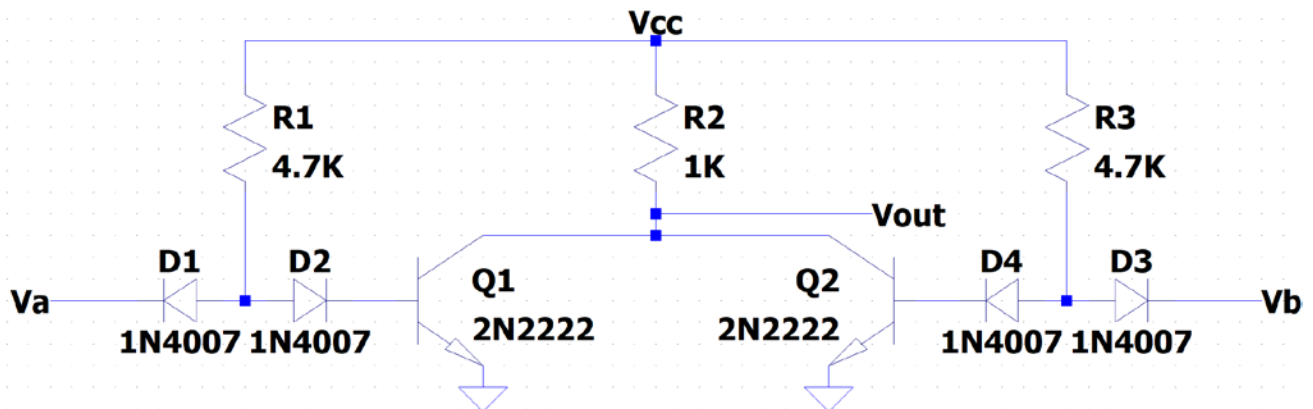


Figure 3-4

Two-input NOR Gate

If all inputs are less than $V_{IL}=V_{BE}(FA)$ then all BJTs are cutoff. AS a result, the output voltage is

$$V_{OH}=V_{CC}$$

If any input is greater than or equal to $V_{BE}(FA)$, the corresponding BJT conduct and if any input reaches V_{IH} $V_{BE}(SAT)$ the output drops to

$$V_{OL} = V_{CE}(SAT)$$

❖ The OR gate

The DTL OR gate combines the DTL NOR gate with DTL inverter. Figure 5 shows a two-input OR gate.

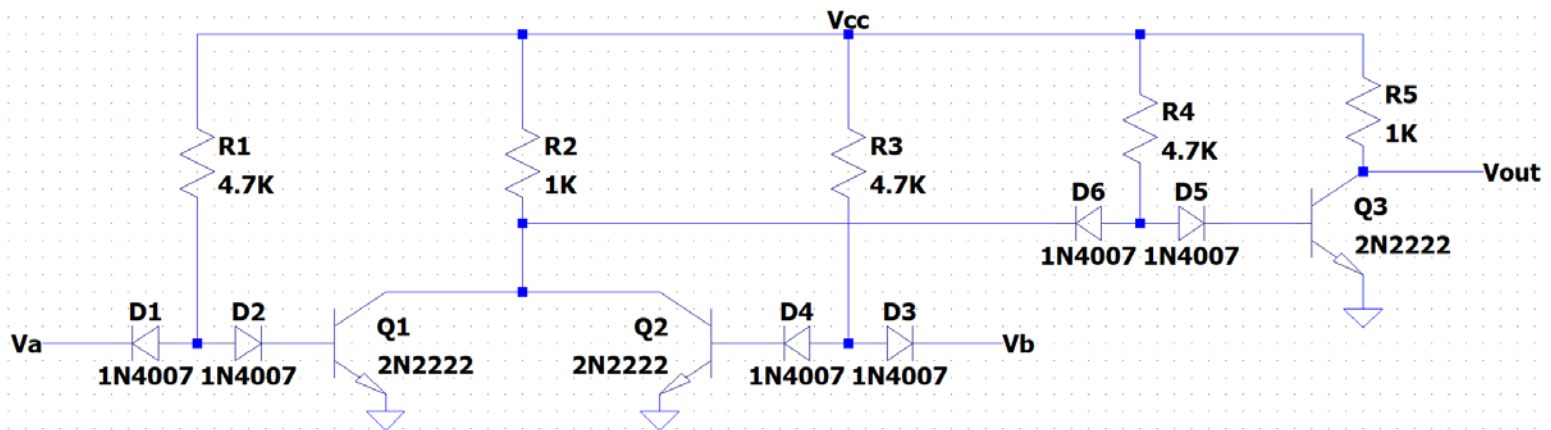


Figure 3-5

Two-input OR Gate

If all inputs are less than $V_{IL}=V_{BE}(FA)$, the transistors are cut-off and the output is

$$V_{OL} = V_{CE}(SAT)$$

If any input is greater than or equal to V_{IL} $V_{BE}(FA)$, the corresponding BJT conduct and if any input reaches $V_{IH}=V_{BE}(SAT)$ the output

$$V_{OH} = V_{CC}$$

Experimental Procedure & Report tasks:

Note: don't forget to write your comments

Note: All the $V_{cc} = 5V$.

♦ Part 1: DTL 2-Input NAND gate:

- 1) Connect the NAND gate circuit shown in Figure (3-2) using LTSpice.
- 2) Investigate its **truth table** by using Transient Analyses.

Attach screenshot showing the circuit and the results.

♦ Part 2: DTL 2-Input AND gate:

1. Using LTSpice find the **VTC** of the circuit shown in Figure (3-3), use DC-Sweep and V_{in} (**0-1V**) then graph V_{out} , attach your schematic with your names written on it.
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♦ Part 3: DTL 2-Input NOR gate:

- 1) Connect the NOR gate circuit shown in Figure (3-4) using LTSpice.
- 2) Investigate its **truth table** by using Transient Analyses.

Attach screenshot showing the circuit and the results.

♦ Part 4: DTL 2-Input OR gate:

1. Using LTSpice find the **VTC** of the circuit shown in Figure (3-5), use DC-Sweep and V_{in} (**0-1V**) then graph V_{out} , attach your schematic with your names written on it.