

Experiment 5

Transistor-Transistor Logic (TTL) Gates

Objectives

- Be familiar with the Transistor -Transistor Logic TTL circuits.
- Studying the internal connection of AND, OR, NAND and NOR.
- To determine the VTC of these gates.
- To find the advantages of this family over DTL family.

Introduction

Looking at the DTL input circuit; we note that the two diodes are opposite to each other in direction. That is, their P_ anodes are connected together and to the pull up resistor, while on cathode is the signal input and the other is connected to the transistor's base. This gives rise to a bit of speculation; could we perhaps replace these two diodes with a single NPN-transistor.

If it works, we can also make use of the fact that the amount space required by a transistor in an IC is essential the same as the space required by a diode. Thus, we can make the IC smaller by eliminating the space required by one of the two diodes

Theoretical Background

❖ The Basic TTL Inverter

Figure 5.1 shows the proposed change to convert a DTL inverter to a Transistor-Transistor logic TTL equivalent. We have merely used one transistor to replace two diodes.

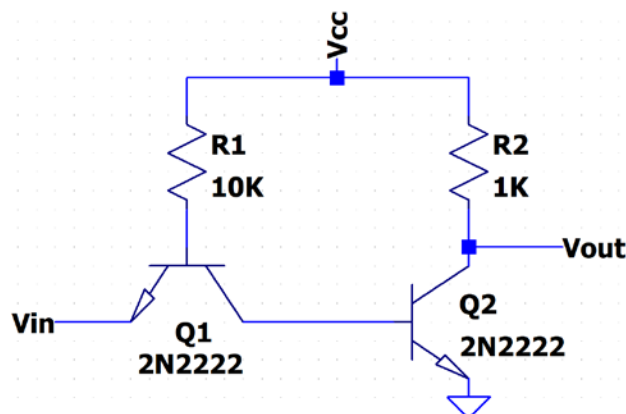


Figure 5.1
TTL inverter

If the input is less than $V_{IL} = V_{BE} - 2(I_{FA}) - V_{CE} - I_{sat}$ then the BJT (Q2) is cutoff. As a result the output voltage is $V_{OH} = V_{CC}$.

If the input is greater than or equal to V_{IL} , the corresponding BJT conduct and if the input reaches $V_{IH} = V_{BE} - 2(I_{sat}) - V_{CE} - I_{sat}$ the output drops to

$$V_{OL} = V_{CE} (sat).$$

❖ The NAND Gate

Figure 5.2 shows a two input TTL NAND gate. A multiple emitter BJT is used to provide the inputs to the gate. A separate BJT could be used for each input with coupled collectors. An advantage of the multiple emitters BJT is that it requires much less chip area than using individual resistors.

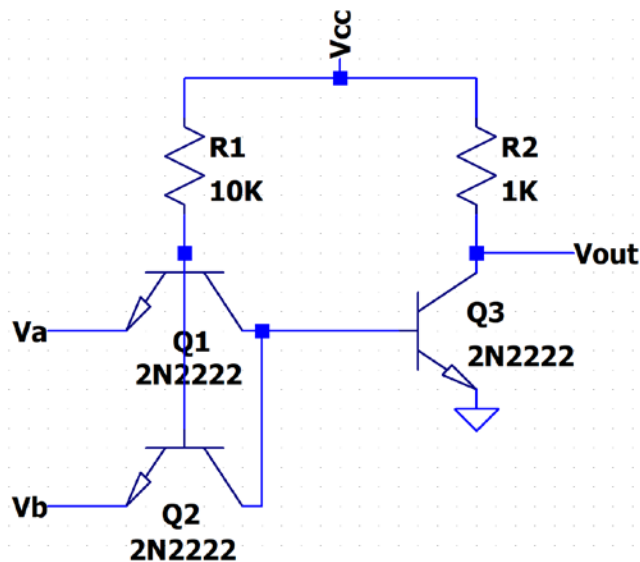


Figure 5.2
2-input NAND Gate

If the input is less than $V_{IL} = V_{BE} - 3(I_{FA}) - V_{CE} - I_{sat}$ then the BJT (Q3) is cutoff. As a result the output voltage is

$$V_{OH} = V_{CC}.$$

If all inputs are greater than or equal to V_{IL} , the BJT (Q3) conduct and if they reach $V_{IH} = V_{BE} - 3(I_{sat}) - V_{CE} - I_{sat}$ the output drops to

$$V_{OL} = V_{CE} (sat).$$

❖ The AND Gate

The TTL AND gate combines the TTL NAND Gate with TTL Inverter.

Figure 5.3 shows a two-input AND Gate.

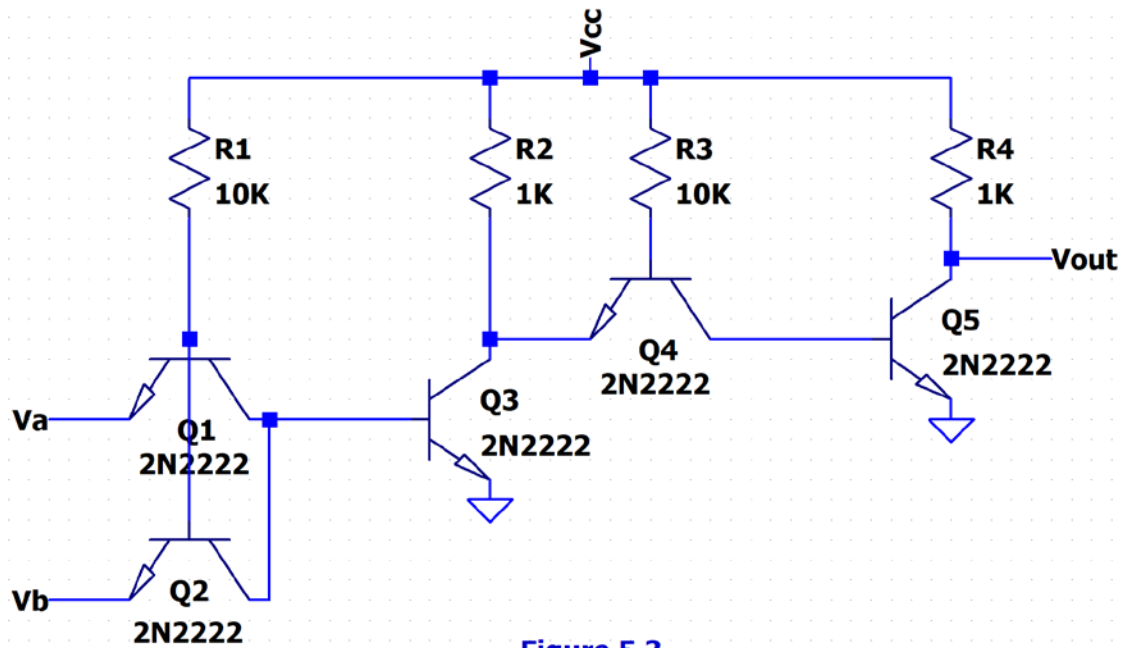


Figure 5.3
2-input AND Gate

if any input is less than $V_{IL} = V_{BE,3(FA)} - V_{CE,1(sat)}$, the transistor Q(3) is cutoff and Q1 is saturated, the output is

$$V_{OL} = V_{CE(sat)}.$$

If all inputs reach $V_{IH} = V_{BE,3(SAT)} - V_{CE,1(sat)}$, the output is

$$V_{OH} = V_{CC}.$$

❖ The NOR Gate

Figure 5.4 shows the schematic diagram of a TTL NOR Gate. As you recall from earlier experiments, it is substantially the same as the RTL and DTL NOR Gates we have already explored. The only difference is that this time we are using the TTL input circuit.

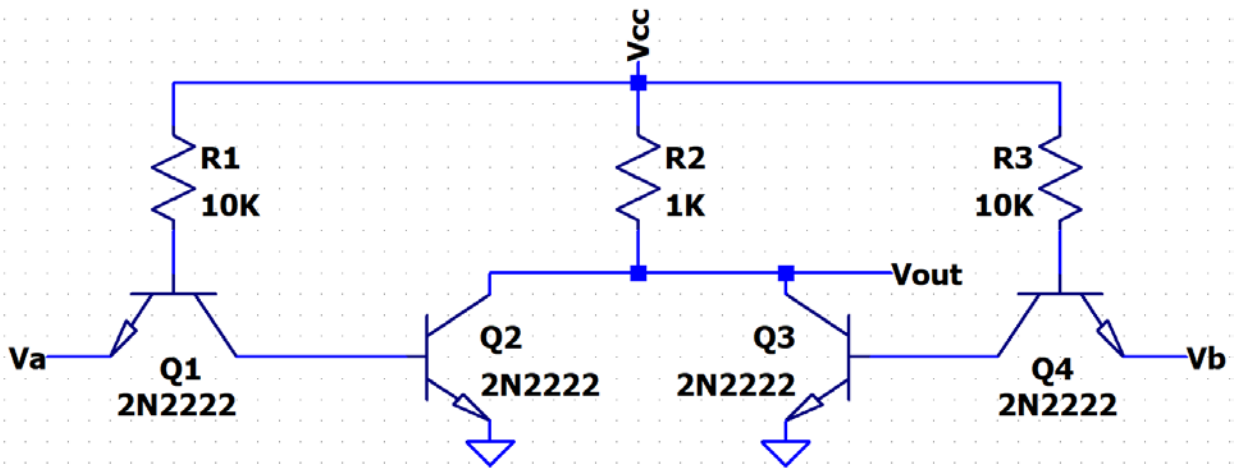


Figure 5.4
2-input NOR Gate

If all inputs are less than $V_{IL} = V_{BE, 2(FA)} - V_{CE, I(sat)}$ then both BJT's (Q2, Q3) is cutoff. As a result the output voltage is

$$V_{OH} = V_{CC}.$$

If any input is greater than or equal to V_{IL} , the corresponding BJT conduct and if it reaches $V_{IH} = V_{BE, 2(sat)} - V_{CE, I(sat)}$ the output drops to

$$V_{OL} = V_{CE} (sat).$$

❖ The OR Gate

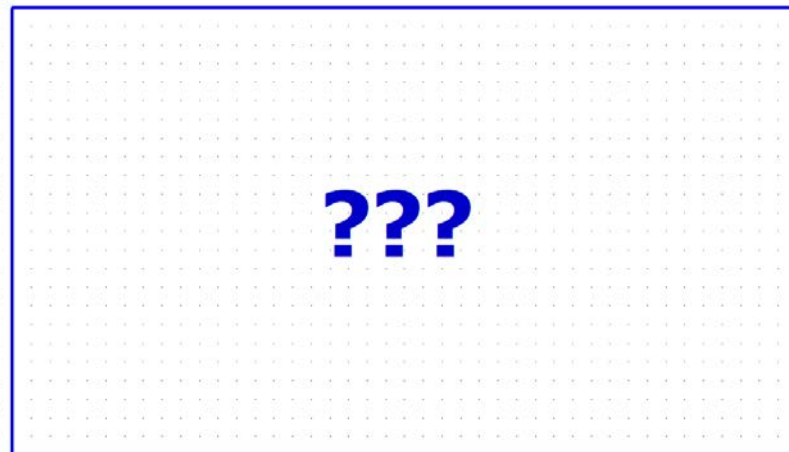


Figure 5.5
2-input OR Gate

Experimental Procedure & Report tasks:

Note: All the $V_{cc} = 5V$.

♦ Part 1: TTL 2-Input AND gate:

1. Using LTspice find the **VTC** of the circuit shown in Figure (5-3), use DC-Sweep and V_{in} (**0.5-0.75V**) then graph V_{out} , attach your schematic.
 - a. Try to use Increment=0.1V and **attach the result**.
 - b. Try to use Increment=0.001V and **attach the result**.
 - c. **What is your comment** on the results above? Does “a” gives real results?

♦ Part 2: TTL 2-Input OR gate:

- 1) From your understanding, **Draw** the TTL 2-input OR gate circuit which is hidden in Figure (5-5) using LTspice.
- 2) Make sure of your circuit by investigating its **truth table** using LTspice Transient Analyses and attach the result.