

Experiment 6

Emitter-Coupled Logic (ECL) Gates

Objectives

- To be familiar with the operation of ECL.
- To determine the VTC of the Inverter and OR/NOR Gates.

Theoretical Background

a) BJT Current Switch

Figure (6.1) shows the ideal BJT current switch. The input is at the base of Q_i , with the base of Q_r held at a constant reference voltage V_{BB} . The coupled emitters are ideally connected to a constant current source I_{EE} .

Outputs are taken at the collector of Q_i and Q_r , giving both inverting and non-inverting outputs:

$$V_{inv} = V_{ci} = V_{cc} - I_{ci} R_{ci}$$

And

$$V_{ninv} = V_{cr} = V_{cc} - I_{cr} R_{cr}$$

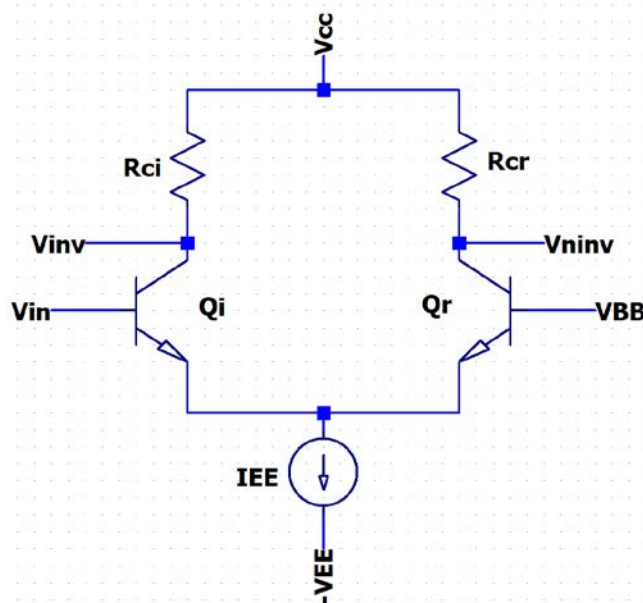


Figure 6.1
Ideal BJT current switch

The states of inverting and non-inverting outputs are determined by whether the input voltage V_{in} is less or greater than the reference voltage V_{BB} . If V_{in} is less than V_{BB} (input low state), the inverting output V_{INV} is the output high state and the non-inverting output V_{NINV} is in the output low state. If V_{in} is greater than V_{BB} (input high state) then V_{INV} is low and V_{NINV} is high.

b) ECL current-switch voltage transfer characteristic

Figure (2) shows the basic ECL inverter and its VTC. Where a resistor R_E is connected between the coupled emitters and $-V_{EE}$. The current I_{RE} is that given by:

$$I_{RE} = (V_E - (-V_{EE})) / R_E.$$

$$V_E = V_{BB} - V_{BE}(ECL)$$

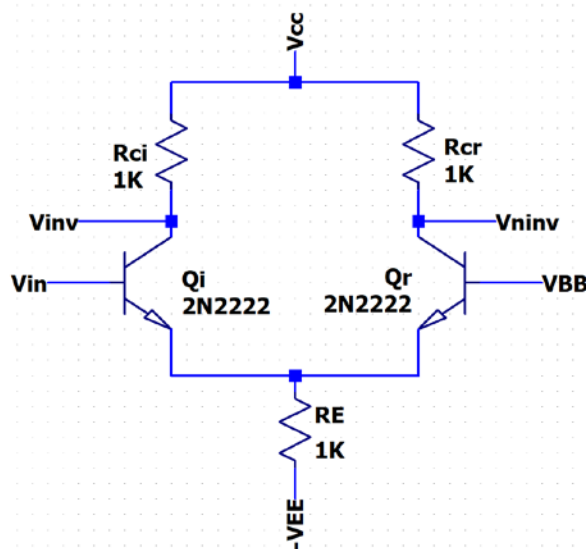


Figure 6.2
Basic ECL inverter

- With $V_{in} < V_{BB}$, Q_i is off and Q_r is in the forward active region of operation; then

$$V_{inv} = V_{CC} = V_{OH}$$

$$V_{ninv} = V_{CC} - I_E * R_{cr} = V_{OL}$$

$$I_{RE} = [V_{BB} - V_{BE}(ECL) + V_{EE}] / R_E$$

- With $V_{in} = V_{BB}$, Q_i and Q_r are both active

$$V_{inv} = V_{ninv} = V_{CC} - I_C * R_C.$$

$$I_C = [(V_{BB} - V_{BE}(ECL) + V_{EE}) / (2 * R_E)]$$

For V_{in} slightly less than V_{BB} Q_i is forward active but not conducting as heavily as Q_r . For V_{in} slightly greater than V_{BB} , Q_r is still on but not conducting as heavily as Q_i . The transition width between V_{IL} and V_{IH} is very narrow. The transition width is found to be approximately:

$$VTW = 0.1V \text{ and centered about } V_{in} = V_{BB}.$$

$$V_{IL} = V_{BB} - 0.05V$$

$$V_{IH} = V_{BB} + 0.05V$$

- With $V_{in} > V_{BB}$, Q_r is off and Q_i is in the forward active region of operation; then

$$V_{inv} = V_{CC} - I_{RE} * R_{cr} = V_{OL}$$

$$V_{ninv} = V_{CC} = V_{OH}$$

$$I_{RE} = (V_{in} - V_{BE}(ECL) + V_{EE}) / R_E$$

- Q_i will eventually saturate with further increases of the input

$$V_s = \frac{V_{CC} + V_{BC}(sat) + \frac{R_{CI}}{R_E} (V_{BE}(sat) - V_{EE})}{1 + \frac{R_{CI}}{R_E}}$$

And

$$V_{in} = V_s, \quad V_{inv} = V_s - V_{BC}(sat)$$

c) Basic ECL NOR/OR Gate

By adding additional input transistors with coupled collectors and coupled emitters to the ECL current switch, the inverting output becomes a NOR outputs and the non-inverting output becomes an OR output.

1. First Configuration

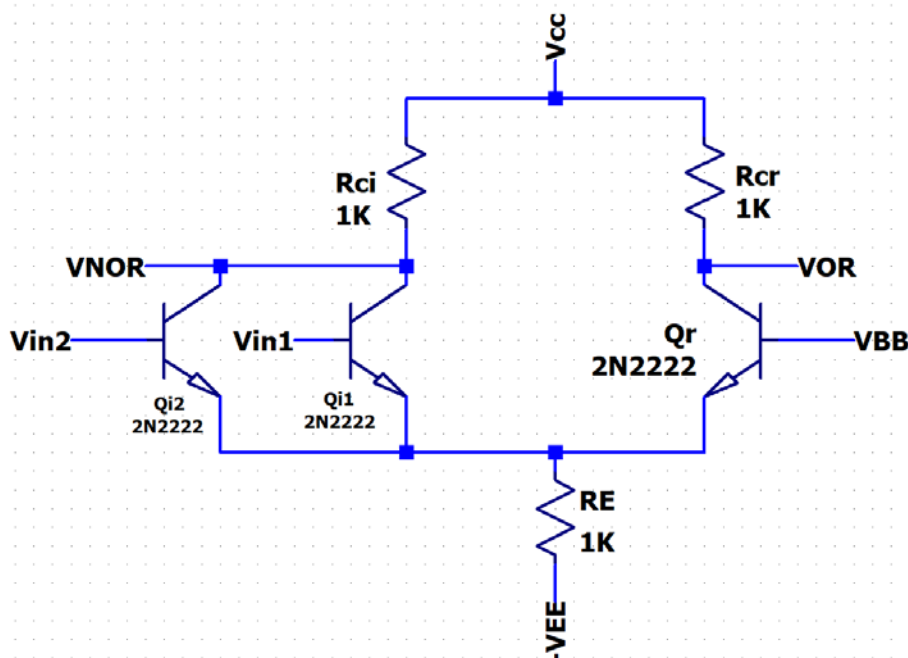


Figure 6.3
Basic ECL OR/NOR Gate

2. Second Configuration

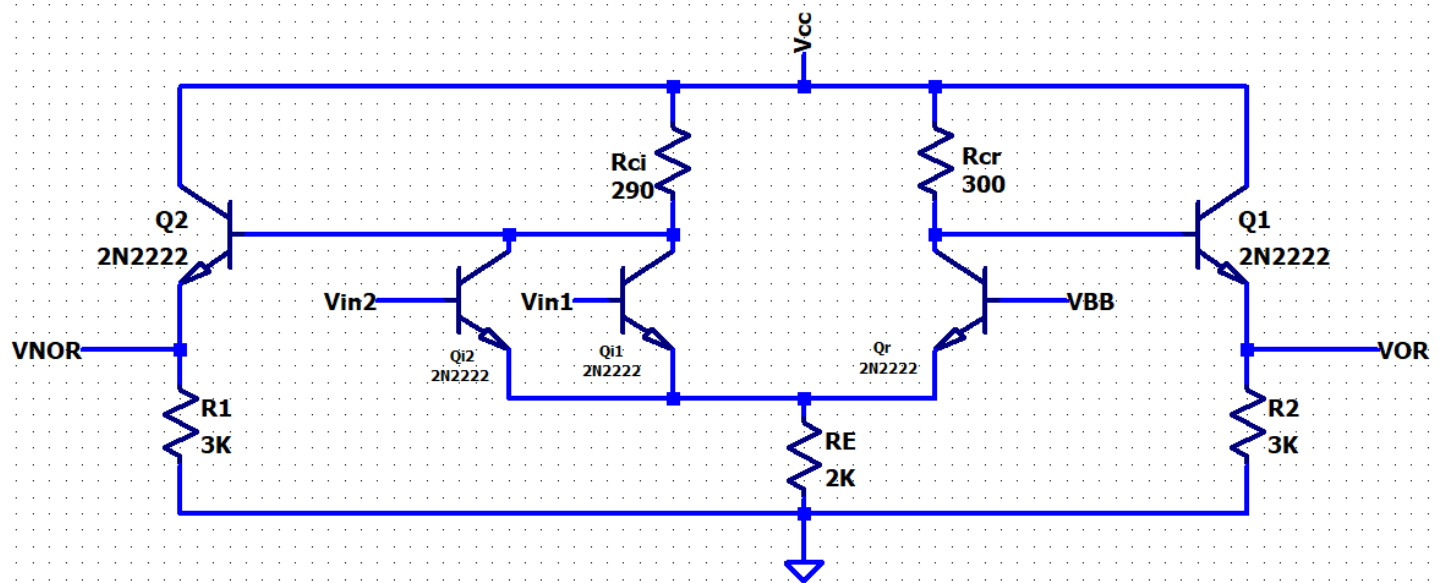


Figure 6.4
Second Configuration for OR/NOR Gate

Experimental Procedure & Report tasks:

Note: Use: $V_{CC} = 5V$, $V_{EE} = 0V$ (GND), $V_{BB} = 2.5V$.

♦ Part 1: Basic ECL inverter:

1. Using LTspice find the **VTC** of the circuit shown in **Figure (6-2)**, use DC-Sweep and V_{in} (**0-5V**) then graph V_{INV} and V_{NINV} on the same graph, attach your schematic and the result.
2. Determine the following:

V_{il}	
V_{ih}	
V_{ol}	
V_{oh}	
V_s	

♦ Part 2: Second Configuration of NOR/OR Gate:

1. Using LTspice find the **VTC** of the circuit shown in **Figure (6-4)**, use DC-Sweep and V_{in} (**0-5.2V**) then graph V_{OR} and V_{NOR} on the same graph, attach your schematic and the result.
2. Determine the following:

V_{il}	
V_{ih}	
V_{ol}	
V_{oh}	
V_s	

3. Draw I_{Rcr} in another plot pane and attach the result.