

Experiment 7

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

Objectives

- To be familiar with the operation of N-MOSFET.
- To study:
 1. Resistor Loaded N-MOSFET Inverter.
 2. Saturated Enhancement only loaded N-MOSFET Inverter.

Theoretical Background

I. N-MOSFET Operation

In order for drain current flow from drain to source in an N-Channel MOSFET, the gate to source voltage must be greater than the specific device voltage (V_T), and the drain to source voltage must be greater than zero.

The threshold voltage is dependent upon the physical dimensions and parameters for the MOSFET device. For the enhancement only N-MOSFET transistor the threshold voltage is positive, and for the enhancement depletion, the threshold voltage is negative.

Regions of Operations

- **Cutoff** → $V_{gs} < V_T$

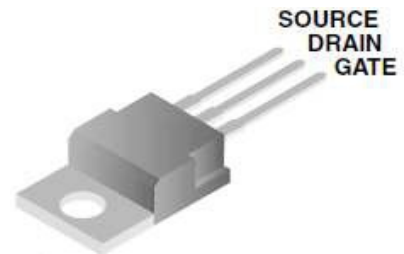
$$I_{D(OFF)} = 0$$

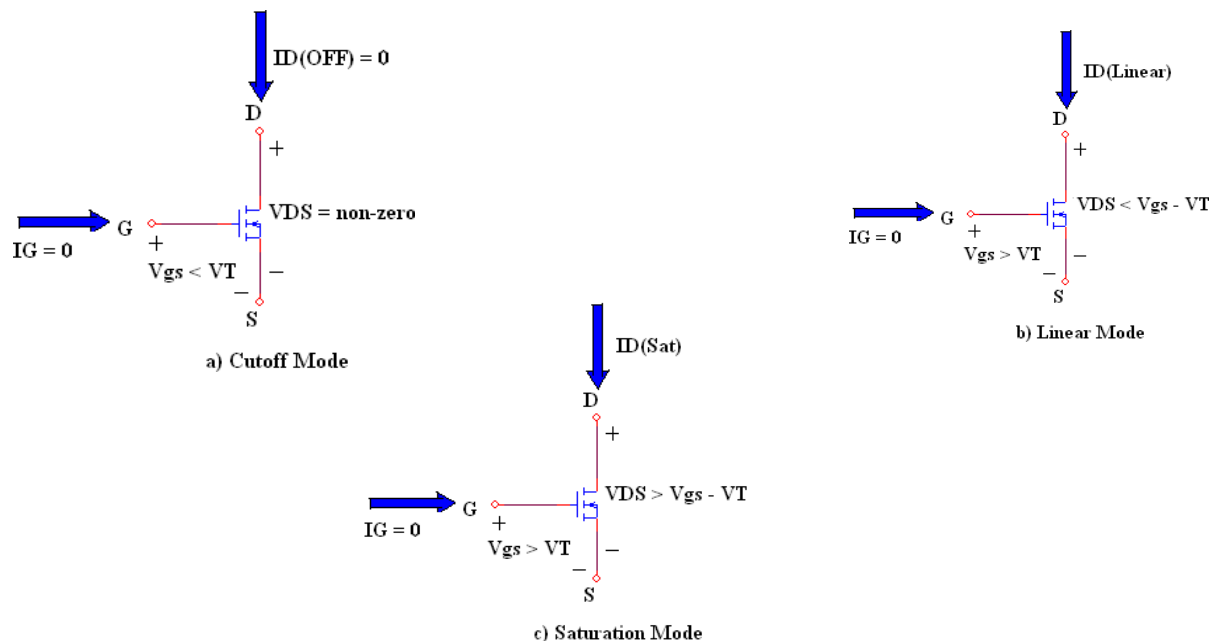
- **Linear** → $V_{GS} > V_T$ and $V_{GS} - V_T > V_{DS}$

$$I_{D(linear)} = k[(V_{GS} - V_T)V_{DS} - (V_{DS}^2)/2]$$

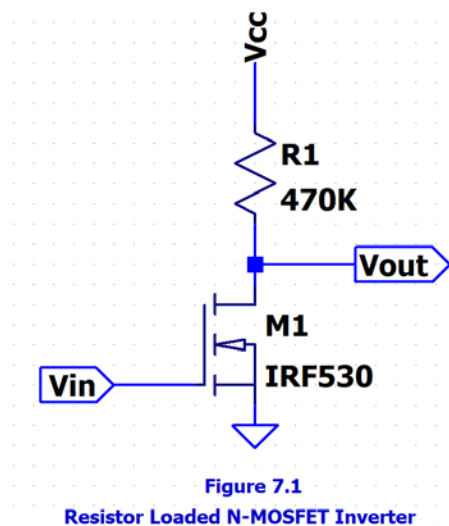
- **Saturation** → $V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T$

$$I_{D(sat)} = (k/2)(V_{GS} - V_T)^2$$





1. Resistor Loaded N-MOSFET Inverter:



Calculations of VTC critical points for resistor loaded N-Mos Inverter:

- **Output high voltage V_{oh} :**

When $V_{gs} < V_T$ then $V_{out} = V_{oh} = V_{DD}$.

- **Output low voltage V_{ol} :**

In the output low state M1 is in linear region of operation

$$V_{OL} = \frac{V_{DD}}{KRL(V_{DD} - V_T) + 1}$$

- **Input low voltage V_{il} :**

$$V_{IL} = V_T + \frac{1}{KRL}$$

- **Input high voltage V_{IH}** (solve the following equation to find V_{IH}):

$$3 \frac{k}{8} (V_{IH} - V_T)^2 + \frac{1}{2R_L} (V_{IH} - V_T) - \frac{V_{DD}}{R_L} = 0$$

- **Midpoint Voltage V_M** (solve the following equation to find V_M):

$$\frac{k}{2} V_M^2 + \left(\frac{1}{R_L} - kV_T \right) V_M + \left(\frac{k}{2} V_T^2 - \frac{V_{DD}}{R_L} \right) = 0$$

- **Static Power Dissipation $P_{DD}(avg)$:**

$$P_{DD}(avg) = \frac{I_{dd}(OL) \times V_{DD}}{2}$$

- **Dynamic Power Dissipation $P_{DD}(dyn)$:**

$$P_{DD}(dyn) = CL \times v \times V_{DD}^2$$

2. Saturated Enhancement Only Loaded N-Mos Inverter:

Calculation of VTC critical points for saturated enhancement only loaded N-Mos Inverter.

- **Output high voltage V_{OH} :**

$$V_{OH} = V_{DD} - V_{T,L}$$

- **Input low voltage V_{IL} :**

$$V_{IL} = V_{T,O}$$

- **Output low voltage V_{OL} :**

$$V_{OL} \approx \frac{k_L (V_{DD} - V_{T,L})^2}{2k_L (V_{DD} - V_{T,L}) + 2k_O (V_{DD} - V_{T,L} - V_{T,O})}$$

- **Input high voltage V_{IH} :**

$$V_{IH} = V_{T,O} + \frac{2(V_{DD} - V_{T,L})}{\sqrt{\frac{3k_O}{k_L}} + 1}$$

- **Midpoint voltage V_M :**

$$V_M = \frac{V_{DD} - V_{T,L} + \sqrt{\frac{k_O}{k_L}} V_{T,O}}{1 + \sqrt{\frac{k_O}{k_L}}}$$

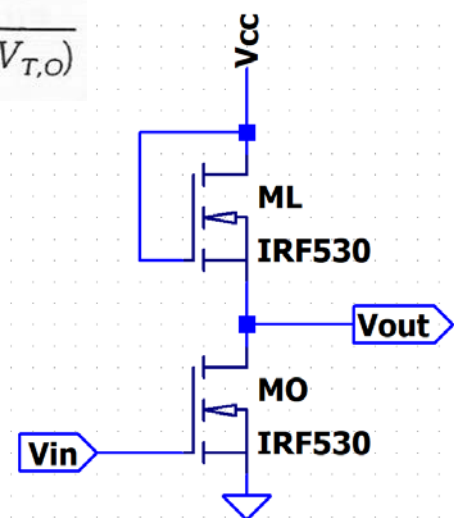


Figure 7.2

Saturated Enhancement Only Loaded N-Mos Inverter

Experimental Procedure & Report tasks:

Note: Use: $V_{CC} = 5V$.

Note: Pay attention to the scaling factors of the units of measurement (m, μ , n).

◆ Part 1: Resistor Loaded N-MOSFET Inverter:

1. Using LTspice find the **VTC** of the circuit shown in **Figure (7-1)**, use DC-Sweep and V_{in} (**0-5V**) then graph V_{out} , attach your schematic and the result.
2. Determine the following:

V_{il}	
V_{ih}	
V_{ol}	
V_{oh}	

3. Graph IR1 when { V_{in} (**0-5V**) with 0.001V increment} and { V_{cc} (**0-10V**) with 2V increment}.

◆ Part 2: Saturated Enhancement Only Loaded N-Mos Inverter:

1. Using LTspice find the **VTC and Power dissipation of ML** of the circuit shown in **Figure (7-2)**, use DC-Sweep and V_{in} (**0-5V**) then graph V_{out} , attach your schematic and the result.
2. Try to change **ML** to **NMOS** model, what are the differences happened to the VTC and Power dissipation of ML? what is your comment?