

Experiment 8

N-MOS Gates

Objectives

- Be familiar with logic gates using resistors and N-MOSFET Transistor.
- Studying the internal connection of AND, OR, NAND, and NOR.
- To determine the VTC of these gates.

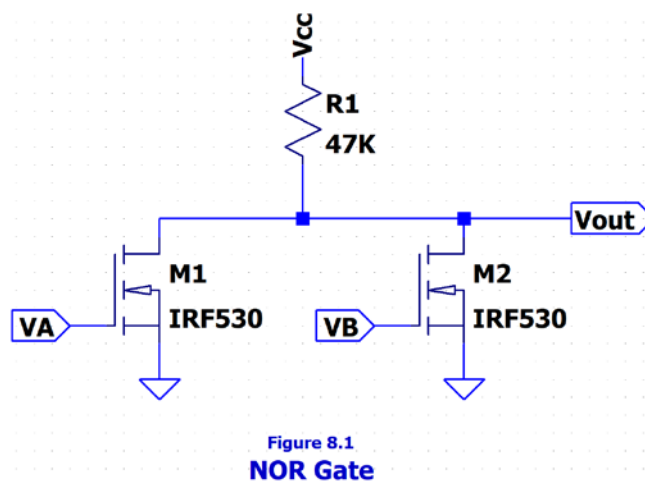
Theoretical Background

The previous Experiment described NMOS logic families and their implantation in inverter form.

In the present Experiment is dedicate to describing the design of Multi-input NMOS logic gates such as NANDs, NORs, AND, OR inverters.

I. NMOS NOR GATE:

The general NMOS inverter can be augmented to perform the logical NOR function by placing additional out put NMOS transistors in parallel with the output N-Channel MOSFET. **Figure 8.1** shows a two input NMOS NOR gate with a generic load. Both NMOS transistors have their drain-to-source channels connected from the output to ground.



- **Output High Voltage VoH:**

If both inputs to the NMOS gate of **Figure 8.1** are low, both output transistor (M1 & M2) will be cutoff.

$$V_{oh} = V_{DD}$$

- **Output Low Voltage VoL:**

If any input is high, results in an output low voltage. The parallel output NMOS structure is referred to as a parallel pull-down , since it is construction of several possible pull-down paths from the output to ground.

$$V_{ol} = \frac{V_{DD}}{K_{RL}(V_{DD} - V_T) + 1}$$

- **Input Low and High Voltage ViL & ViH:**

The input low and high voltage for NMOS logic family NOR Gates are the same as those for corresponding inverter.

$$V_{il} = V_T + \frac{1}{K_{RL}}$$

$$\frac{3K}{8}(V_{ih} - V_T)^2 + \frac{1}{2RL}(V_{ih} - V_T) - \frac{V_{DD}}{RL}$$

II. NMOS NAND GATE:

NAND gates can also be easily constructed using NMOS circuitry **Figure 8.2**, shows a two input NMOS NAND gate with a generic load.

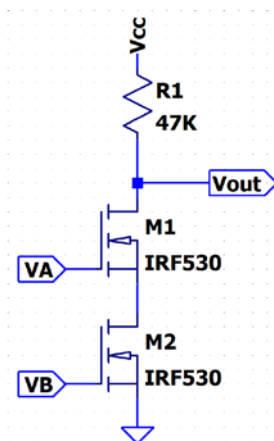


Figure 8.2
NAND Gate

- **Output High Voltage VoH:**

An output high voltage is obtained from the NMOS NAND gates of Figure 9.2 for either input being low.

- **Output Low Voltage VoL:**

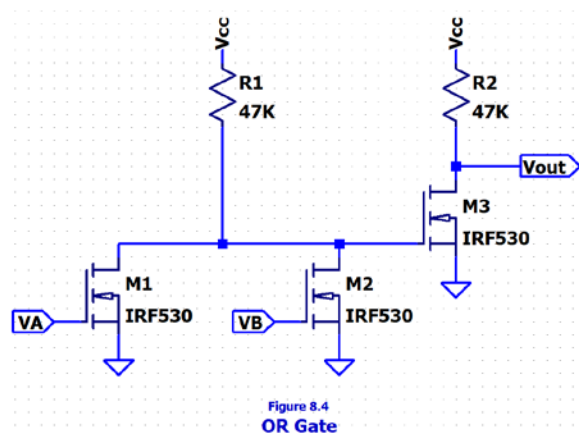
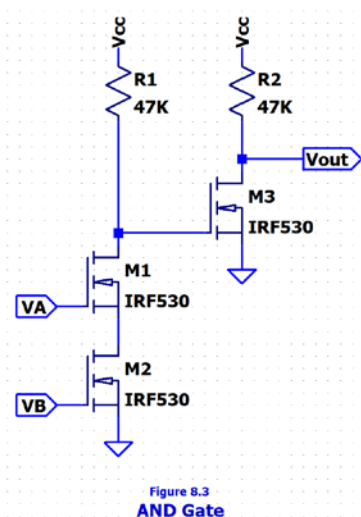
An output low voltage is obtained from the NMOS NAND gates of Figure 9.2 for both inputs being high.

- **Input Low and High Voltage V_{iL} & V_{iH} :**

The input low and high voltage for NMOS logic family inverter are all dependent on K_o and increase in V_{oL} can also be used to show change in V_{iL} and V_{iH} for each of the logic family.

III. NMOS OR & AND GATES:

OR and AND gates are obtained using NMOS logic families by simply connecting inverters to the outputs of NOR and NAND gates, respectively. **Figure 8.3** and **Figure 8.4**, show NMOS OR and AND gates with generic load.



Experimental Procedure & Report tasks:

Note: Use: $V_{CC} = 5V$.

♦ Part 1: N-MOS NOR Gate:

1. Using LTspice find the **VTC** of the circuit shown in **Figure (8-1)**, use DC-Sweep and V_{in} (**3-4.5V**) then graph V_{out} , attach your schematic and the result.
2. Determine the following:

V_{il}	
V_{ih}	
V_{ol}	
V_{oh}	

♦ Part 2: Combined logic gates:

1. Using the circuits we learned in the Experiment and using the inverter gate we learned in Lab7, construct the following circuit and **attach the schematic of it**:

$\text{Out} = AB + B'$

2. Find the truth table of this circuit, **fill the values in the following table**:

A	B	B'	AB	AB+B'
0	0			
0	1			
1	0			
1	1			

3. Find the truth table for the circuit **using Transient analyses**.