



The Islamic University of Gaza

Faculty of Engineering

Department of Computer Engineering

Digital Electronics LAB

[LAB 04]

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Supervisor

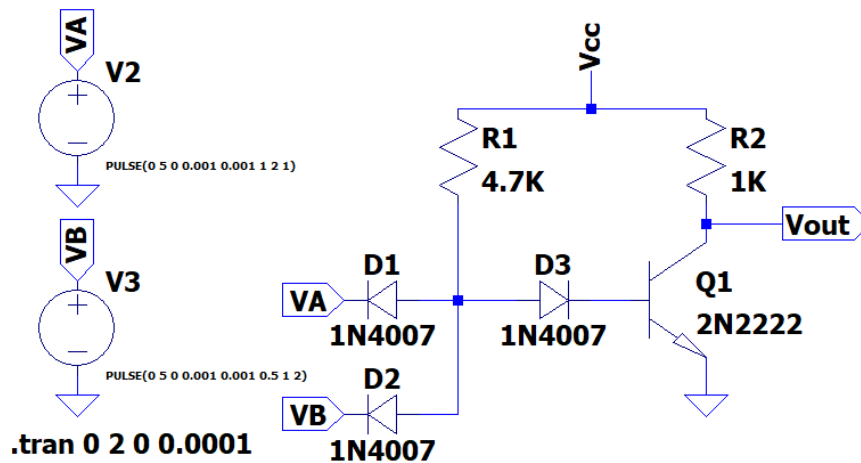
Eng. Saja Nabeel Nabhan

❖ Objectives:

- Be familiar with the diode-transistor logic DTL circuit.
- Studying the internal connection of AND, OR, NAND, and NOR.
- To determine the VTC of these gates.
- To find the advantages of this family over the RTL family.

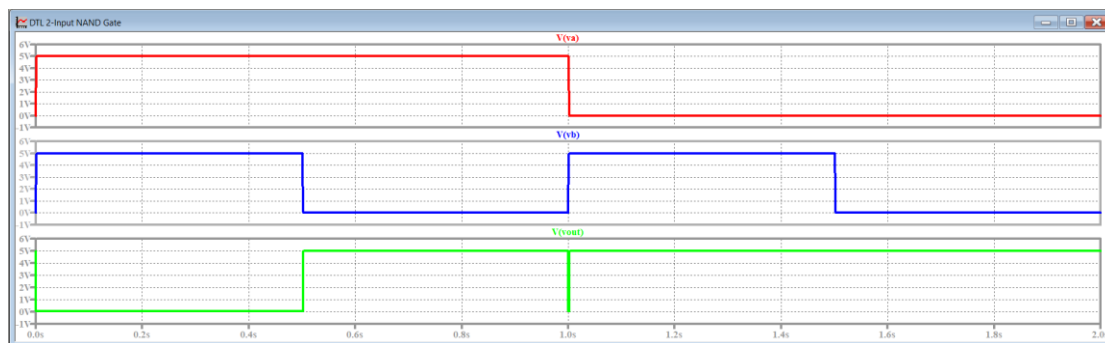
❖ Part (1): DTL 2-Input NAND gate:

A. Connect the NAND gate circuit shown in Figure (3-2) using LTSpice.



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B. Investigate its **truth table** by using Transient Analyses.

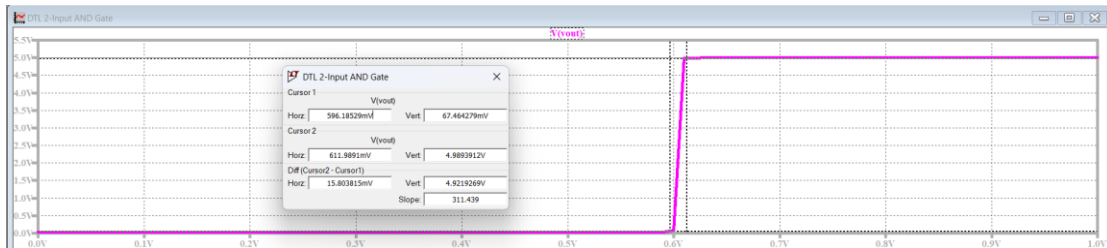
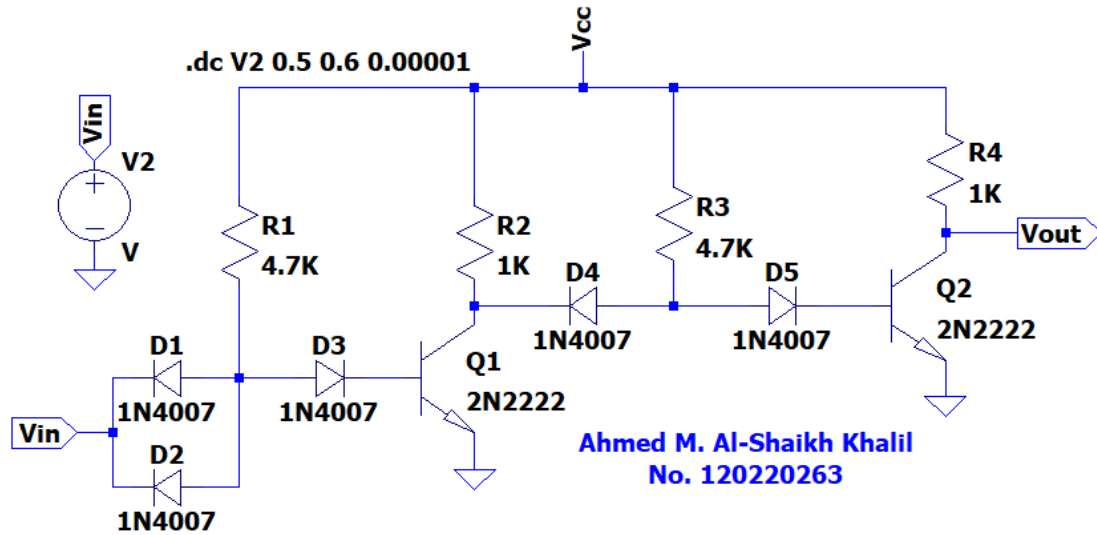


Using the graphical representation, we can write the truth table as follows:

V_A	V_B	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

❖ Part (2): DTL 2-Input AND gate:

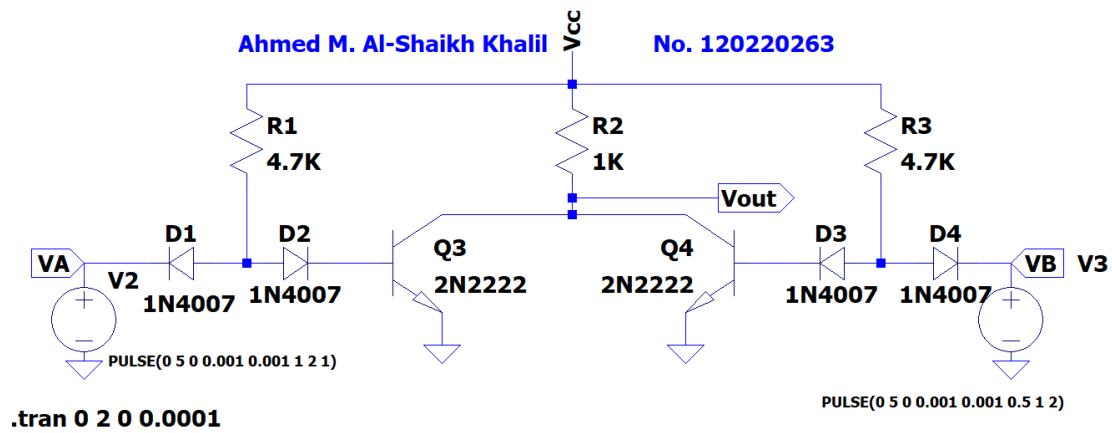
A. Using LTSpice find the VTC of the circuit shown in Figure (3-3), use DC-Sweep and Vin (0-1V) then graph Vout, attach your schematic with your names written on it.



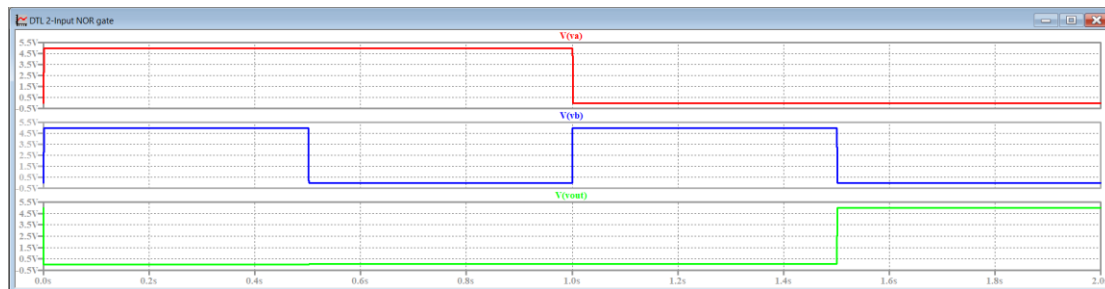
V_{IL}	596.18529mV
V_{IH}	611.9891mV
V_{OH}	4.9893912V
V_{OL}	67.464279mV

❖ Part (3): DTL 2-Input NOR gate:

A. Connect the NOR gate circuit shown in Figure (3-4) using LTSpice.



B. Investigate its **truth table** by using Transient Analyses.

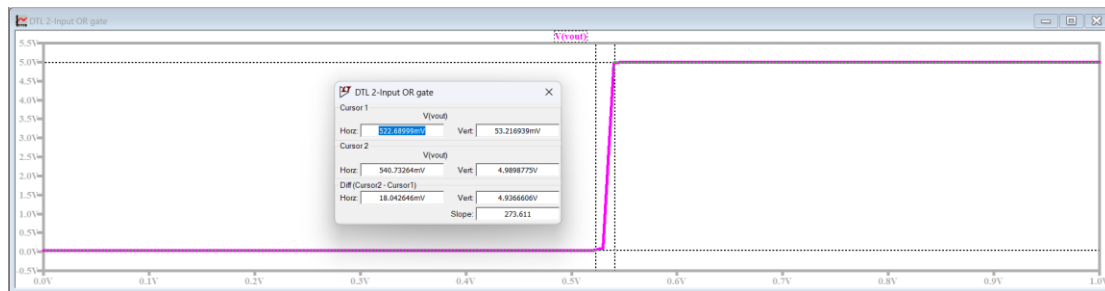
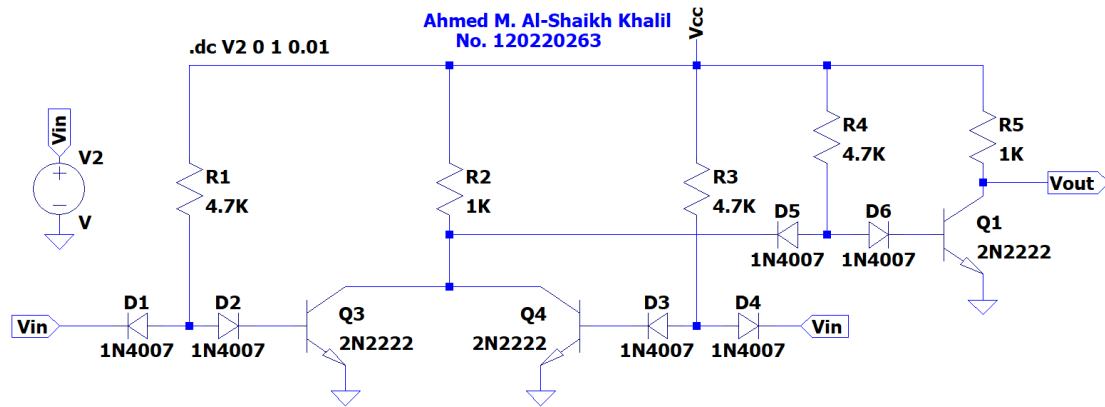


Using the graphical representation, we can write the truth table as follows:

V_A	V_B	V_{out}
1	1	0
1	0	0
0	1	0
0	0	1

❖ Part (4): DTL 2-Input OR gate:

A. Using LTSpice find the **VTC** of the circuit shown in Figure (3-5), use DC-Sweep and V_{in} (**0-1V**) then graph V_{out} , attach your schematic with your names written on it.



V_{IL}	522.68999mV
V_{IH}	540.73264mV
V_{OH}	4.9898775V
V_{OL}	53.216939mV