



The Islamic University of Gaza

Faculty of Engineering

Department of Computer Engineering

Digital Electronics Lab

[Lab05]

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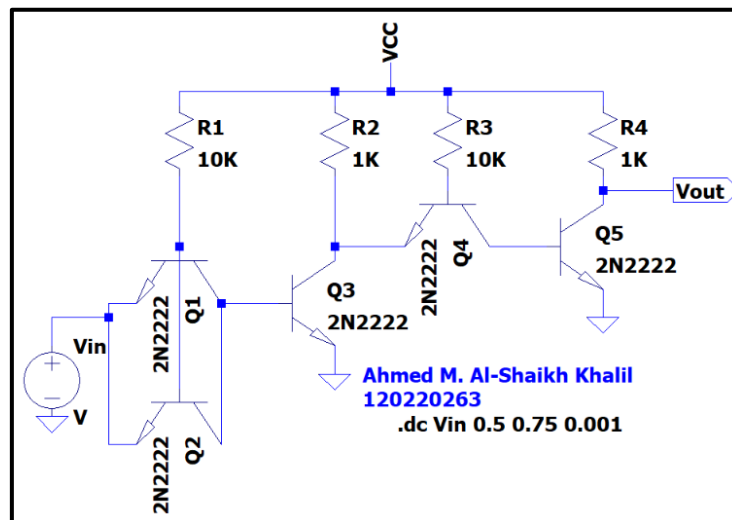
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❖ Objectives

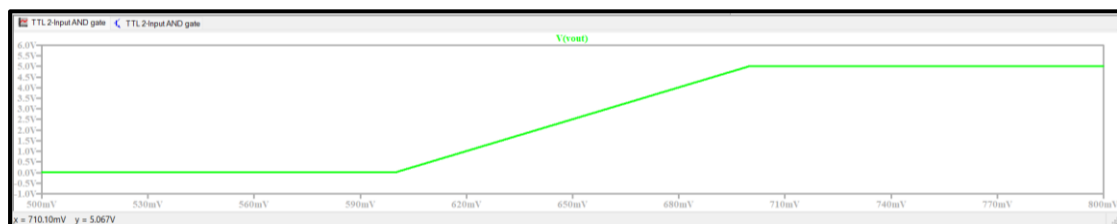
- Be familiar with the Transistor -Transistor Logic TTL circuits.
- Studying the internal connection of AND, OR, NAND and NOR.
- To determine the VTC of these gates.
- To find the advantages of this family over DTL family.

❖ Part (1): TTL 2-Input AND gate:

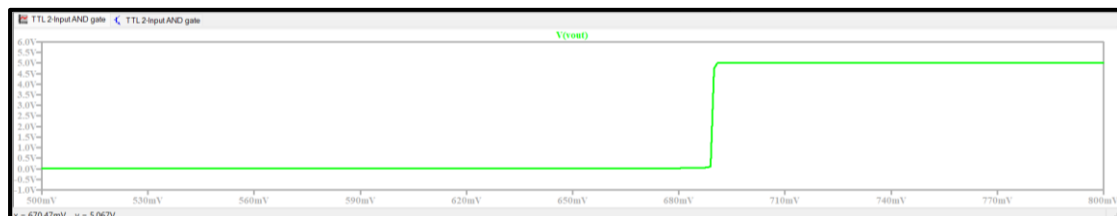
A. Using LTspice find the **VTC** of the circuit shown in Figure (5-3), use DC-Sweep and **Vin (0.5-0.8V)** then graph Vout, attach your schematic.



a. Try to use Increment = 0.1V and attach the result.



b. Try to use Increment = 0.001V and attach the result.



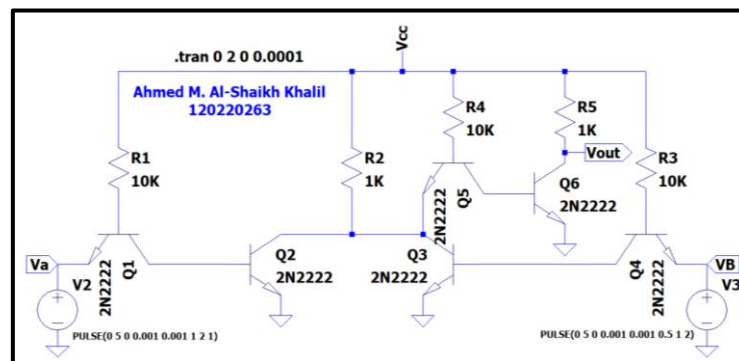
c. What is your comment on the results above? Does “a” gives real results?

Plot (a) is not accurate because the step size (0.1V) is too large and misses the sharp transition.

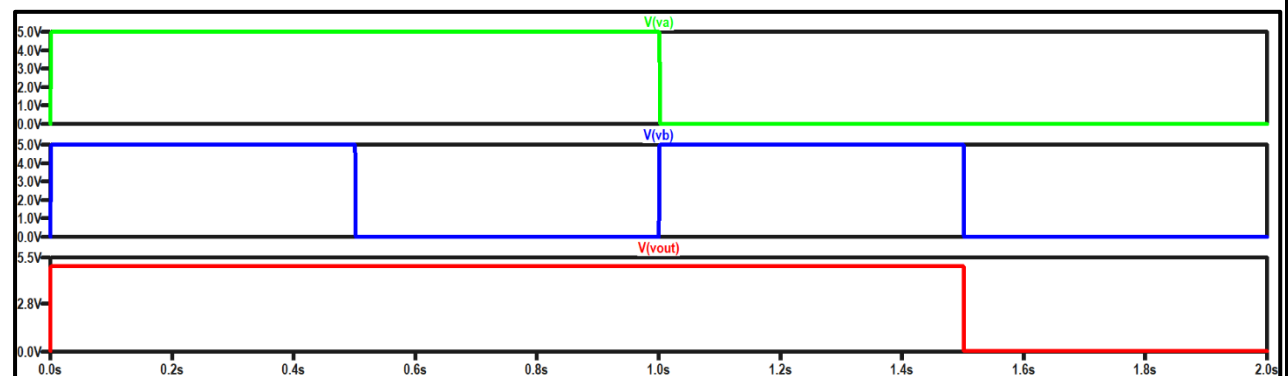
Plot (b) with a small step (0.001V) gives the correct and real VTC result.

❖ Part (2): TTL 2-Input OR gate:

A. From your understanding, **Draw** the TTL 2-input OR gate circuit which is hidden in Figure (5-5) using LTspice.



B. Make sure of your circuit by investigating its **truth table** using LTspice Transient Analyses and attach the result.



Using the graphical representation, we can write the truth table as follows:

V_A	V_B	V_{out}
1	1	1
1	0	1
0	1	1
0	0	0

❖ Conclusion

This experiment provided a comprehensive analysis of the **Transistor-Transistor Logic (TTL)** family and its operational principles within logic gates. By focusing on the 2-input **AND gate** circuit, the following insights were concluded:

- **TTL Architecture:** The effectiveness of the TTL family in implementing logic gates stems from its reliance on transistors at both the input and output stages, ensuring robust switching performance.
- **Precision in DC Sweep Analysis:** Through the use of **LTspice** to obtain the **Voltage Transfer Characteristics (VTC)**, it was observed that the step size (Increment) is critical for accuracy.
 - A large increment (0.1V) proved insufficient as it failed to capture the sharp transitions in the curve.
 - Reducing the increment to 0.001V resulted in a significantly smoother and more accurate VTC, revealing the precise behavior of the gate during state changes.
- **Input-Output Relationship:** The study clarified the direct relationship between input and output voltages, allowing for a better understanding of noise margins and logic level thresholds.

❖ Summary

To obtain realistic and reliable results in circuit simulation, using a small increment in DC Sweep analysis is essential, particularly for capturing high-speed switching characteristics. Overall, TTL remains a fundamental technology in digital electronics due to its transistor-driven logic stages.