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Faculty of Engineering

Department of Computer Engineering

Digital Electronics Laboratory

[Lab 07]

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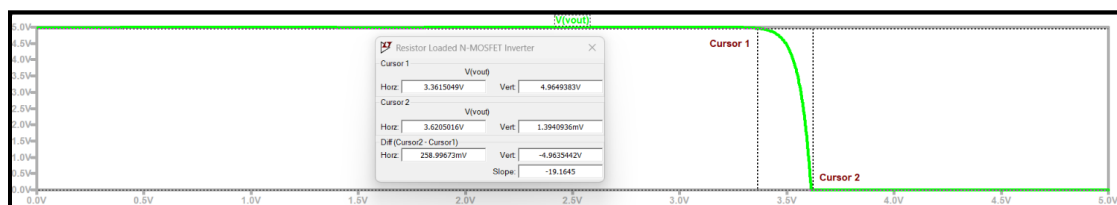
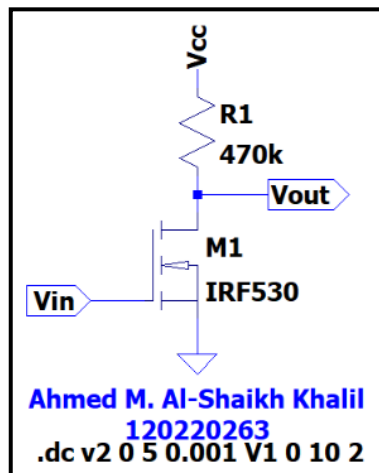
Eng. Saja Nabhan

❖ Objectives

- To be familiar with the operation of N-MOSFET.
- To study:
 1. Resistor Loaded N-MOSFET Inverter.
 2. Saturated Enhancement only loaded N-MOSFET Inverter.

❖ Part (1): Resistor Loaded N-MOSFET Inverter:

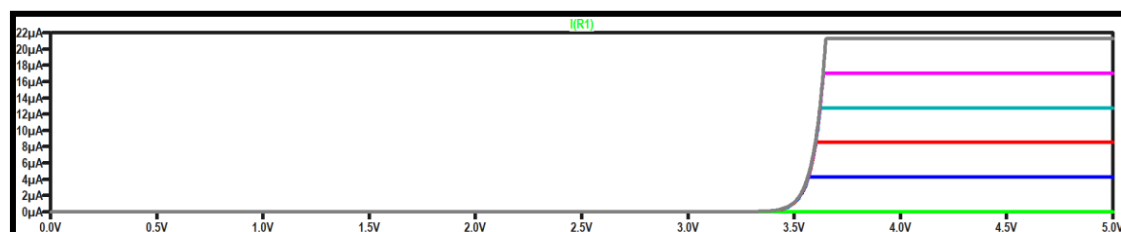
A. Using LTspice find the **VTC** of the circuit shown in **Figure (7-1)**, use DC-Sweep and **Vin (0-5V)** then graph **Vout**, attach your schematic and the result.



B. Determine the following:

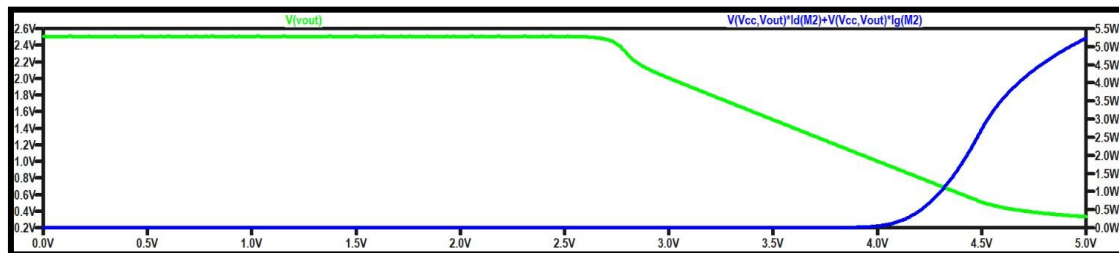
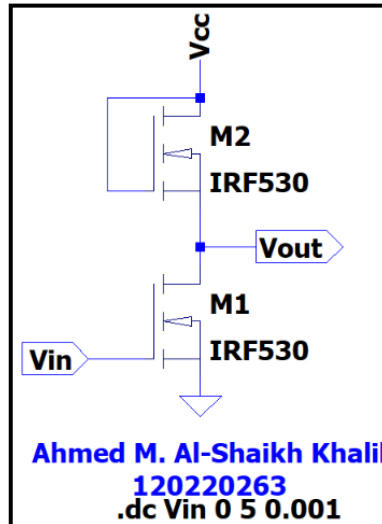
V_{il}	3.3615049V
V_{ih}	3.6205016V
V_{ol}	1.3940936mV
V_{oh}	4.9649383V

C. Graph IR1 when {**Vin (0-5V)** with 0.001V increment} and {**Vcc (0-10V)** with 2V increment}.

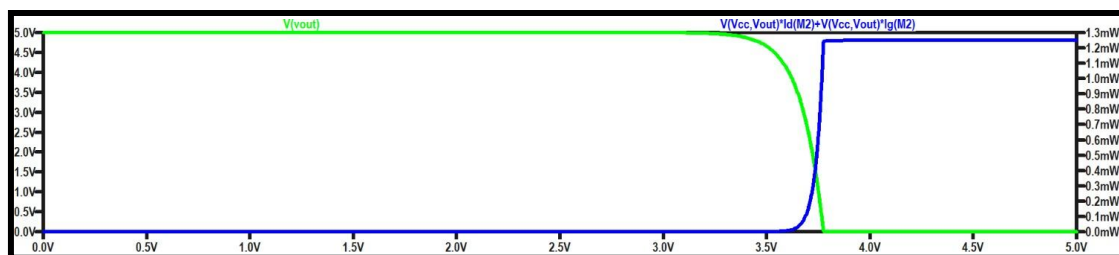


❖ Part (2): Saturated Enhancement Only Loaded N-Mos Inverter:

A. Using LTspice find the **VTC** and **Power dissipation of ML** of the circuit shown in **Figure (7-2)**, use DC-Sweep and **Vin (0-5V)** then graph **Vout**, attach your schematic and the result.



B. Try to change ML to NMOS model, what are the differences happened to the VTC and Power dissipation of ML? what is your comment?



The experimental data indicates a substantial variation in the VTC slope and power metrics upon altering the MOSFET type. The original device exhibits a slow, near-linear degradation of the output voltage, while the newly selected MOSFET introduces a significantly steeper drop-off, implying a tighter noise margin and higher sensitivity. Architecturally, this transition yields a monumental reduction in power expenditure, successfully shrinking the power dissipation from approximately 5 W to roughly 1.3mW, thereby verifying the efficacy of the new component selection.