

Experiment 9

C-MOS Gates

Objectives

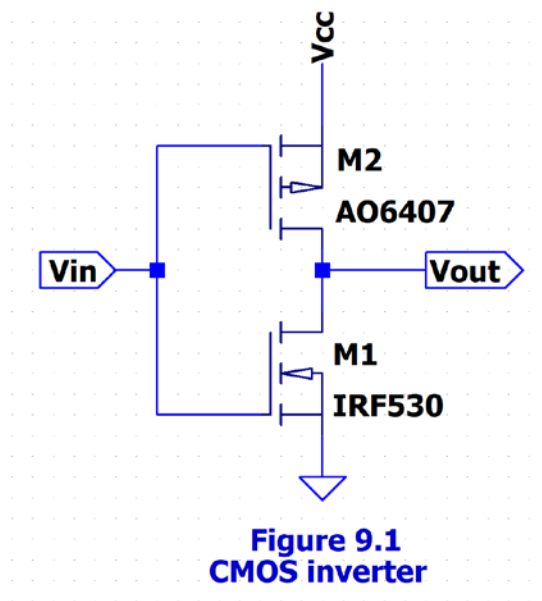
- To be familiar with the operation of CMOS Logic Gates.
- To determine the VTC of these gates.

Theoretical Background

Complementary MOS or CMOS is a logic family that uses N-channel and P-channel MOSFETs. In this family a PMOS is used as a pull-up load device, while NMOS as a pull down device.

1. CMOS Inverter:

Figure 9.1 shows a CMOS inverter with P-channel and N-channel MOSFETs.



- **Output High State:**

If the input voltage is low, NMOS transistor will be off with $I_{D,N} = I_{D,P} = 0$, so the output voltage is equal to VDD.

$$V_{OH} = V_{DD}.$$

- **Output Low State:**

For the input voltage equal to VDD or VOH, PMOS is off and $I_{D,N} = I_{D,P} = 0$, and the output voltage will be zero.

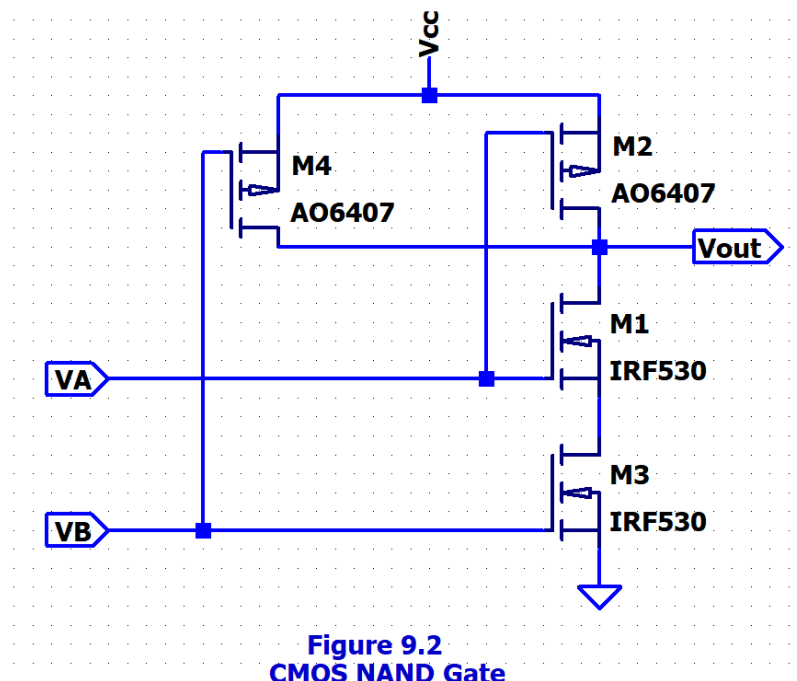
$$V_{OL} = 0.$$

- **Intermediate Voltages:**

- When V_{in} reaches $V_{T,N}$, NMOS turns on and operates in saturation, while PMOS still is in active region. "Input Low State"
- As V_{in} increases, V_o begins to reduce causing $V_{DS,N}$ to drop, in this case NMOS enters a linear region. When V_o drops to $-V_{T,P}$, PMOS enters a saturation mode. "Input high state"
- At the midpoint voltage where $V_{in} = V_o = V_M$, both NMOS and PMOS operate in saturation mode.

2. CMOS NAND Gate:

Figure 9.2 shows a two input CMOS NAND gate, output pull-up is provided by two PMOS in parallel connections, while two NMOS with series connection provide an output pull-down to ground.



- **Output High State:**

This state is obtained by two cases:

- If both inputs are low, the two PMOS are in active operation providing an output pull-up to VDD, while the two NMOS are off, so $I_{D,PA} = I_{D,PB} = 0$, and $V_{DS,PA} = V_{DS,PB} = 0$.
- With a single input low, an output pull up path to VDD exists through the corresponding PMOS, with the corresponding NMOS is off and no current is passed through NMOS.

In each case:

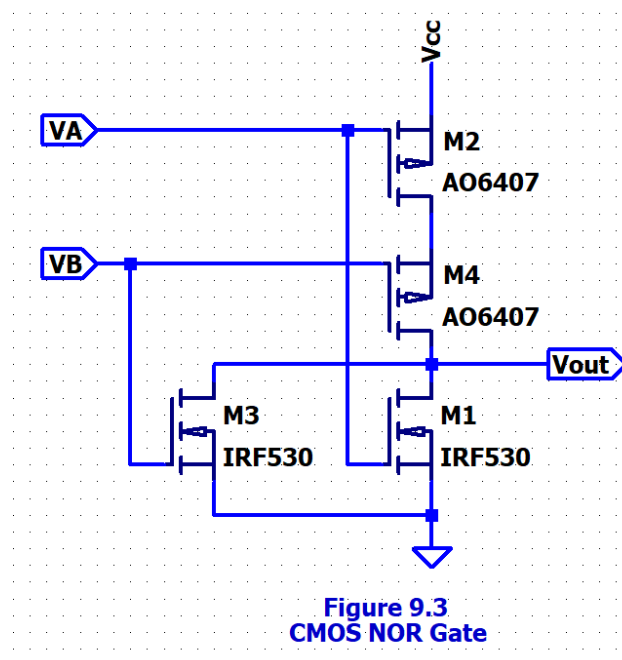
$$V_{OH}=V_{DD}.$$

- **Output Low State:**

This state is obtained only if the two inputs are high as follow, if A and B inputs are high, NA and NB are in active operation, while PA and PB are off, so no output pull up path to VDD is available and the currents $I_{D,NA} = I_{D,NB} = 0$, and $V_{OL}=0$.

3. CMOS NOR Gate:

Figure 9.3 shows a two input CMOS NOR Gate, the NOR function can be obtained with CMOS pairs; PMOS devices in series to provide pull-up configuration and NMOS devices in parallel to provide pull-down configuration.



- **Output Low State:**

The output low can be obtained by two cases:

- If both inputs are high, the gate to source voltage for both NMOS brings them into active operation providing an active pull-down to ground, while PMOS's are off.
- If any input is high the corresponding NMOS is in active operation to provide an output pull-down to ground.

In each case:

$$V_{OL}=0.$$

- **Output High State:**

This state can be occurred only if the two inputs are low, where both NA and NB are off, while the PMOS devices are in active operation to provide an output pull-up to VDD.

$$V_{OH}=V_{DD}$$

Experimental Procedure & Report tasks:

Note: Use: VCC = 5V.

♦ **Part 1: C-MOS NAND Gate:**

1. Using LTspice, find the **Truth table** of the Circuit shown in **Figure (9-2)** using Transient analyses.
2. Find the **VTC** for the same circuit, use DC-Sweep and Vin (**4.1-4.4V**) then graph Vout, attach your schematic and the result.
3. Determine the following:

Vil	
Vih	
Vol	
Voh	
VM	

♦ **Extra Part: C-MOS NOR Gate: (Bonus +2Marks)**

**** Do the same tasks required in Part1 for the NOR gate shown in **Figure (9-3)**.**

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