
Electronics 1

All Problems

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Basic Physics of Semiconductors

PROBLEMS

Sec. 2.1 Semiconductor Materials and Their Properties

2.1. The intrinsic carrier concentration of germanium (GE) is expressed as

$$n_i = 1.66 \times 10^{15} T^{3/2} \exp \frac{-E_g}{2kT} \text{ cm}^{-3}, \quad (2.127)$$

where $E_g = 0.66 \text{ eV}$.

(a) Calculate n_i at 300 K and 600 K and compare the results with those obtained in Example 2.1 for Si.

(b) Determine the electron and hole concentrations if Ge is doped with P at a density of $5 \times 10^{16} \text{ cm}^{-3}$.

2.2. An n -type piece of silicon experiences an electric field equal to $0.1 \text{ V}/\mu\text{m}$.

(a) Calculate the velocity of electrons and holes in this material.

(b) What doping level is necessary to provide a current density of $1 \text{ mA}/\mu\text{m}^2$ under these conditions? Assume the hole current is negligible.

2.3. A n -type piece of silicon with a length of $0.1\ \mu\text{m}$ and a cross section area of $0.05\ \mu\text{m} \times 0.05\ \mu\text{m}$ sustains a voltage difference of 1 V.

- If the doping level is $10^{17}\ \text{cm}^{-3}$, calculate the total current flowing through the device at $T = 300\ \text{K}$.
- Repeat (a) for $T = 400\ \text{K}$ assuming for simplicity that mobility does not change with temperature. (This is not a good assumption.)

2.4. From the data in Problem 2.1, repeat Problem 2.3 for Ge. Assume $\mu_n = 3900\ \text{cm}^2/(\text{V} \cdot \text{s})$ and $\mu_p = 1900\ \text{cm}^2/(\text{V} \cdot \text{s})$.

2.5. Figure 2.37 shows a p -type bar of silicon that is subjected to electron injection from the left and hole injection from the right. Determine the total current flowing through the device if the cross section area is equal to $1\ \mu\text{m} \times 1\ \mu\text{m}$.

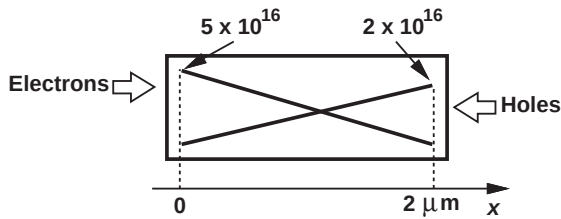


Figure 2.37

2.6. In Example 2.9, compute the total number of electrons “stored” in the material from $x = 0$ to $x = L$. Assume the cross section area of the bar is equal to a .

2.7. Repeat Problem 2.6 for Example 2.10 but for $x = 0$ to $x = \infty$. Compare the results for linear and exponential profiles.

***2.8.** Repeat Problem 2.7 if the electron and hole profiles are “sharp” exponentials, i.e., they fall to negligible values at $x = 2\ \mu\text{m}$ and $x = 0$, respectively (Fig. 2.38).

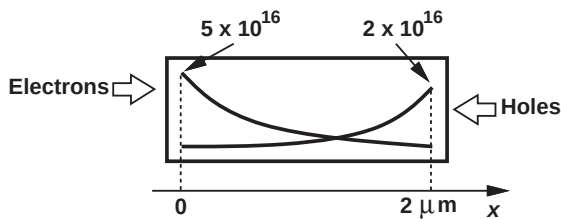


Figure 2.38

2.9. How do you explain the phenomenon of drift to a high school student?

Sec. 2.2 pn Junctions

2.10. A pn junction with $N_D = 3 \times 10^{16}\ \text{cm}^{-3}$ and $N_A = 2 \times 10^{15}\ \text{cm}^{-3}$ experiences a reverse bias voltage of 1.6 V.

- Determine the junction capacitance per unit area.
- By what factor should N_A be increased to double the junction capacitance?

2.11. Due to a manufacturing error, the p -side of a pn junction has not been doped. If $N_D = 3 \times 10^{16}\ \text{cm}^{-3}$, calculate the built-in potential at $T = 300\ \text{K}$.

2.12. A junction employs $N_D = 5 \times 10^{17}\ \text{cm}^{-3}$ and $N_A = 4 \times 10^{16}\ \text{cm}^{-3}$.

- Determine the majority and minority carrier concentrations on both sides.
- Calculate the built-in potential at $T = 250\ \text{K}$, $300\ \text{K}$, and $350\ \text{K}$. Explain the trend.

2.13. An oscillator application requires a variable capacitance with the characteristic shown in Fig. 2.39. Determine N_A and N_D .

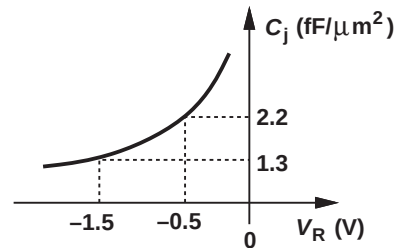


Figure 2.39

***2.14.** Two identical pn junctions are placed in series.

- Prove that this combination can be viewed as a single two-terminal device having an exponential characteristic.
- For a tenfold change in the current, how much voltage change does such a device require?

2.15. Figure 2.40 shows two diodes with reverse saturation currents of I_{S1} and I_{S2} placed in parallel.

- Prove that the parallel combination operates as an exponential device.

- (a) If the total current is I_{tot} , determine the current carried by each diode.

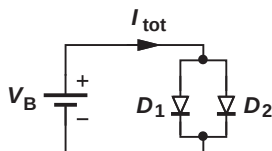


Figure 2.40

- 2.16.** Consider a pn junction in forward bias.
- To obtain a current of 1 mA with a voltage of 750 mV, how should I_S be chosen?
 - If the diode cross section area is now doubled, what voltage yields a current of 1 mA?
- 2.17.** Figure 2.41 shows two diodes with reverse saturation currents of I_{S1} and I_{S2} placed in series. Calculate I_B , V_{D1} , and V_{D2} in terms of V_B , I_{S1} , and I_{S2} .

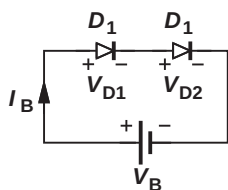


Figure 2.41

- 2.18.** In the circuit of Problem 2.17, we wish to increase I_B by a factor of 10. What is the required change in V_B ?

Sec. 2.2.4 I/V Characteristics

- 2.19.** Consider the circuit shown in Fig. 2.42, where $I_S = 2 \times 10^{-15}$ A. Calculate V_{D1} and I_X for $V_X = 0.5$ V, 0.8 V, 1 V, and 1.2 V. Note that V_{D1} changes little for $V_X \geq 0.8$ V.

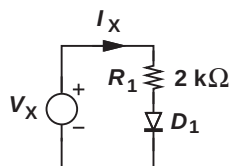


Figure 2.42

- 2.20.** In the circuit of Fig. 2.42, the cross section area of D_1 is increased by a factor of 10. Determine V_{D1} and I_X for $V_X = 0.8$ V and

1.2 V. Compare the results with those obtained in Problem 2.19.

- 2.21.** Suppose D_1 in Fig. 2.42 must sustain a voltage of 850 mV for $V_X = 2$ V. Calculate the required I_S .
- 2.22.** For what value of V_X in Fig. 2.42, does R_1 sustain a voltage equal to $V_X/2$? Assume $I_S = 2 \times 10^{-16}$ A.
- 2.23.** We have received the circuit shown in Fig. 2.43 and wish to determine R_1 and I_S . We note that $V_X = 1$ V $\rightarrow I_X = 0.2$ mA and $V_X = 2$ V $\rightarrow I_X = 0.5$ mA. Calculate R_1 and I_S .

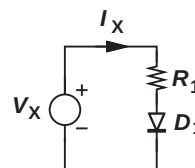


Figure 2.43

- *2.24.** Figure 2.44 depicts a parallel resistor-diode combination. If $I_S = 3 \times 10^{-16}$ A, calculate V_{D1} for $I_X = 1$ mA, 2 mA, and 4 mA.

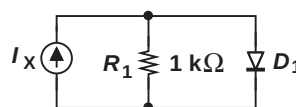


Figure 2.44

- 2.25.** In the circuit of Fig. 2.44, we wish D_1 to carry a current of 0.5 mA for $I_X = 1.3$ mA. Determine the required I_S .
- 2.26.** For what value of I_X in Fig. 2.44, does R_1 carry a current equal to $I_X/2$? Assume $I_S = 3 \times 10^{-16}$ A.
- *2.27.** We have received the circuit shown in Fig. 2.45 and wish to determine R_1 and I_S . Measurements indicate that $I_X = 1$ mA $\rightarrow V_X = 1.2$ V and $I_X = 2$ mA $\rightarrow V_X = 1.8$ V. Calculate R_1 and I_S .

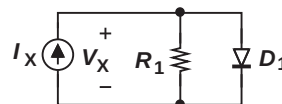


Figure 2.45

- **2.28.** In the circuit of Fig. 2.46, determine the value of R_1 such that this resistor carries 0.5 mA. Assume $I_S = 5 \times 10^{-16}$ A for each diode.

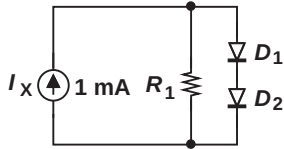


Figure 2.46

- **2.29.** The circuit illustrated in Fig. 2.47 employs two identical diodes with $I_S = 5 \times 10^{-16}$ A. Calculate the voltage across R_1 for $I_X = 2$ mA.

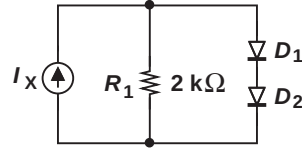


Figure 2.47

- **2.30.** Sketch V_X as a function of I_X for the circuit shown in Fig. 2.48. Assume (a) a constant-voltage model, (b) an exponential model.

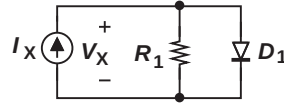


Figure 2.48

SPICE PROBLEMS

In the following problems, assume $I_S = 5 \times 10^{-16}$ A.

- 2.31.** For the circuit shown in Fig. 2.49, plot V_{out} as a function of I_{in} . Assume I_{in} varies from 0 to 2 mA.

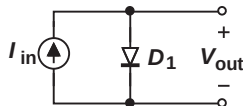


Figure 2.49

- 2.32.** Repeat Problem 2.31 for the circuit depicted in Fig. 2.50, where $R_1 = 1$ k Ω . At what value of I_{in} are the currents flowing through D_1 and R_1 equal?

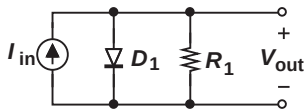


Figure 2.50

- 2.33.** Using SPICE, determine the value of R_1 in Fig. 2.50 such that D_1 carries 1 mA if $I_{in} = 2$ mA.

- 2.34.** In the circuit of Fig. 2.51, $R_1 = 500$ Ω . Plot V_{out} as a function of V_{in} if V_{in} varies from -2 V to $+2$ V. At what value of V_{in} are the voltage drops across R_1 and D_1 equal?

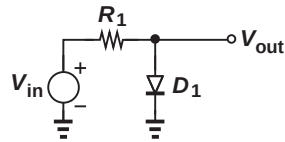


Figure 2.51

- 2.35.** In the circuit of Fig. 2.51, use SPICE to select the value of R_1 such that $V_{out} < 0.7$ V for $V_{in} < 2$ V. We say the circuit “limits” the output.

REFERENCE

1. B. Streetman and S. Banerjee, *Solid-State Electronic Device*, fifth edition, Prentice-Hall, 1999.

Diode Models and Circuits

PROBLEMS

In the following problems, assume $V_{D,on} = 800 \text{ mV}$ for the constant-voltage diode model.

Section 3.2 *pn* Junction as a Diode

- 3.1.** Plot the I/V characteristic of the circuit shown in Fig. 3.63.

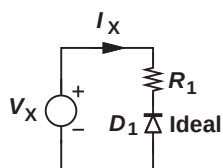


Figure 3.63

- 3.2.** If the input in Fig. 3.63 is expressed as $V_X = V_0 \cos \omega t$, plot the current flowing through the circuit as a function of time.
- 3.3.** Plot I_X as a function of V_X for the circuit shown in Fig. 3.65 for two cases: $V_B = -1 \text{ V}$ and $V_B = +1 \text{ V}$.

- 3.4.** For the circuit depicted in Fig. 3.64, plot I_X as a function of V_X for two cases: $V_B = -1 \text{ V}$ and $V_B = +1 \text{ V}$.

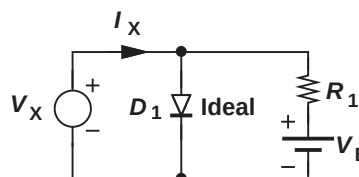


Figure 3.64

- 3.5.** If in Fig. 3.65, $V_X = V_0 \cos \omega t$, plot I_X as a function of time for two cases: $V_B = -1 \text{ V}$ and $V_B = +1 \text{ V}$.

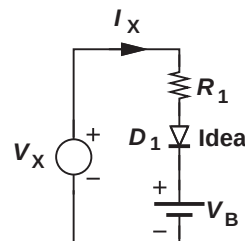


Figure 3.65

- 3.6.** Plot I_X and I_{D1} as a function of V_X for the circuit shown in Fig. 3.66. Assume $V_B > 0$.

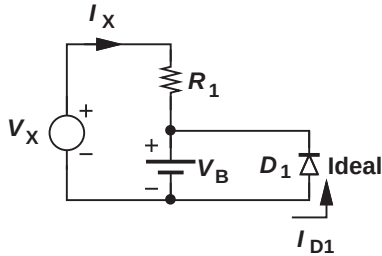


Figure 3.66

- 3.7.** In the circuit of Fig. 3.67, plot I_X and I_{R1} as a function of V_X for two cases: $V_B = -1$ V and $V_B = +1$ V.

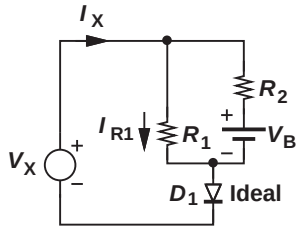


Figure 3.67

- 3.8.** For the circuit depicted in Fig. 3.68, plot I_X and I_{R1} as a function of V_X for two cases: $V_B = -1$ V and $V_B = +1$ V.

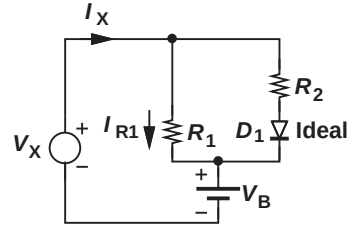


Figure 3.68

- *3.9.** Plot the input/output characteristics of the circuits depicted in Fig. 3.69 using an ideal model for the diodes. Assume $V_B = 2$ V.

- *3.10.** Repeat Problem 3.9 with a constant-voltage diode model.

- *3.11.** If the input is given by $V_{in} = V_0 \cos \omega t$, plot the output of each circuit in Fig. 3.69 as a function of time. Assume an ideal diode model.

- **3.12.** Plot the input/output characteristics of the circuits shown in Fig. 3.70 using an ideal model for the diodes.

- **3.13.** Repeat Problem 3.12 with a constant-voltage diode model.

- **3.14.** Assuming the input is expressed as $V_{in} = V_0 \cos \omega t$, plot the output of each circuit in Fig. 3.70 as a function of time. Use an ideal diode model.

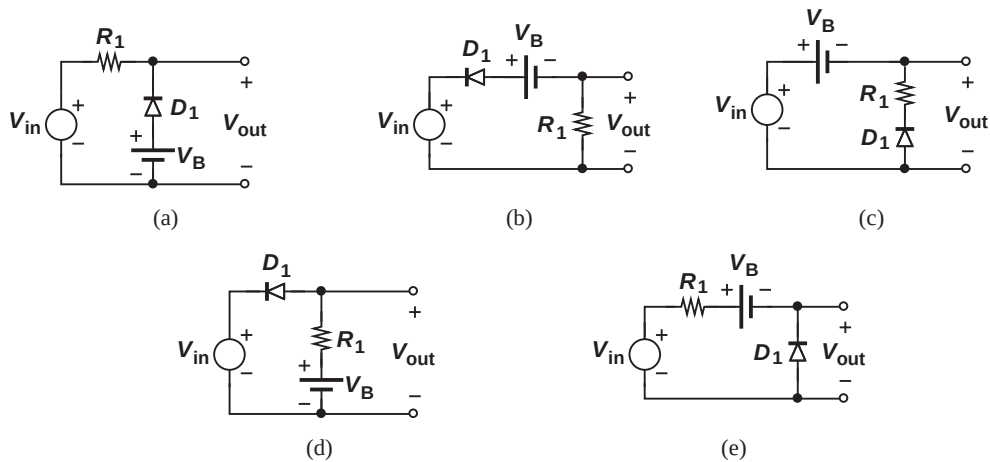


Figure 3.69

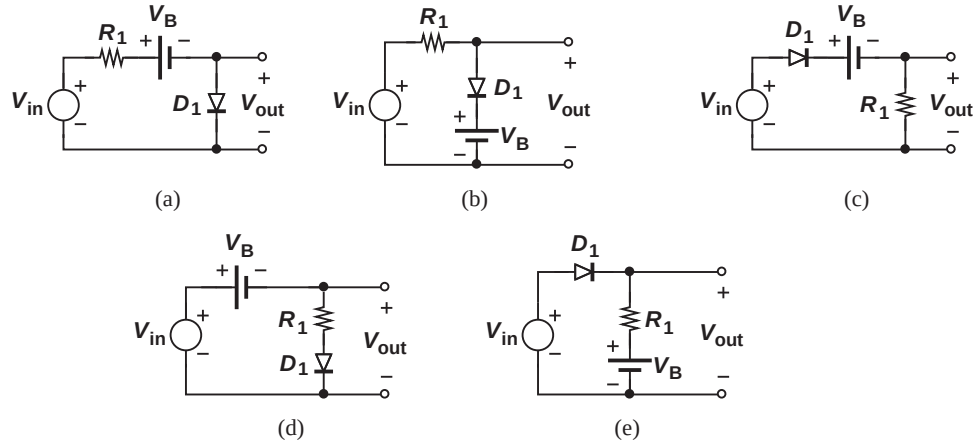


Figure 3.70

- **3.15.** Assuming a constant-voltage diode model, ****3.17.** For the circuits illustrated in Fig. 3.71, plot V_{out} as a function of I_{in} for the circuits shown in Fig. 3.71.
- **3.16.** In the circuits of Fig. 3.71, plot the current flowing through R_1 as a function of V_{in} . Assume a constant-voltage diode model. ****3.18.** Plot V_{out} as a function of I_{in} for the circuits shown in Fig. 3.72. Assume a constant-voltage diode model.

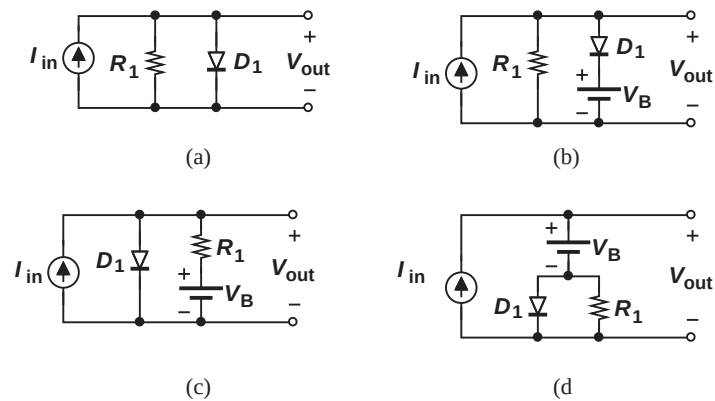


Figure 3.71

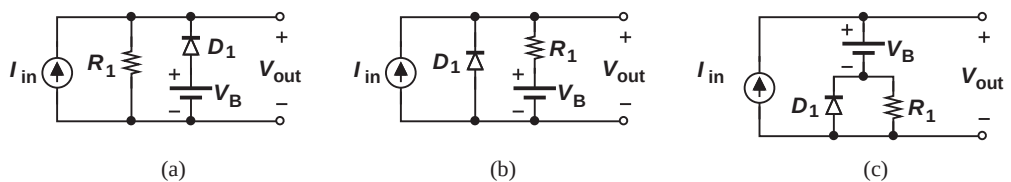


Figure 3.72

- *3.19.** Plot the current flowing through R_1 in the circuits of Fig. 3.72 as a function of I_{in} . Assume a constant-voltage diode model.
- *3.20.** In the circuits depicted in Fig. 3.72, assume $I_{in} = I_0 \cos \omega t$, where I_0 is relatively large. Plot V_{out} as a function of time using a constant-voltage diode model.
- *3.21.** For the circuits shown in Fig. 3.73, plot V_{out} as a function of I_{in} assuming a constant-voltage model for the diodes.
- *3.22.** Plot the current flowing through R_1 as a function of I_{in} for the circuits of Fig. 3.73. Assume a constant-voltage diode model.

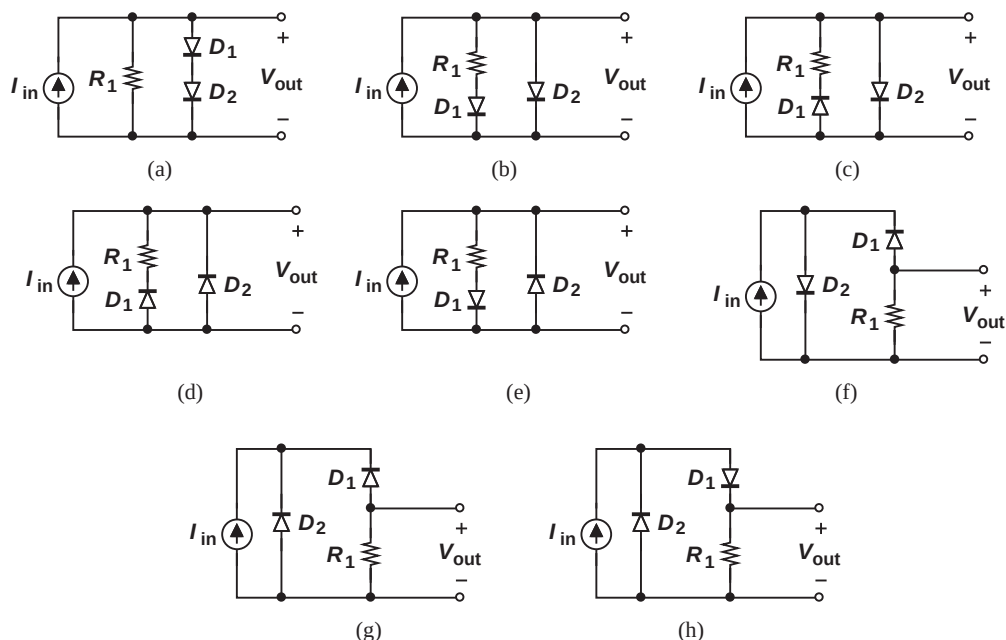


Figure 3.73

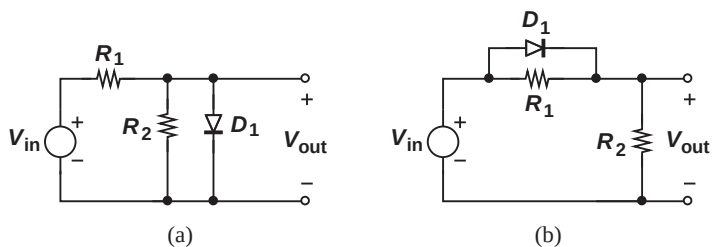


Figure 3.74

- *3.23.** Plot the input/output characteristic of the circuits illustrated in Fig. 3.74 assuming a constant-voltage model.
- *3.24.** Plot the currents flowing through R_1 and D_1 as a function of V_{in} for the circuits of Fig. 3.74. Assume a constant-voltage diode model.
- *3.25.** Plot the input/output characteristic of the circuits illustrated in Fig. 3.75 assuming a constant-voltage model.
- *3.26.** Plot the currents flowing through R_1 and D_1 as a function of V_{in} for the circuits of Fig. 3.75. Assume a constant-voltage diode model.

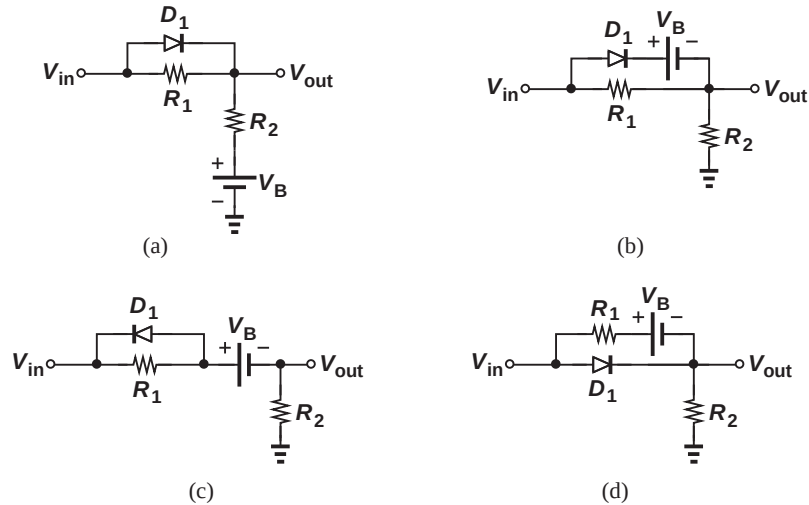


Figure 3.75

- **3.27.** Plot the input/output characteristic of the circuits illustrated in Fig. 3.76 assuming a constant-voltage model and $V_B = 2$ V.
- **3.28.** Plot the currents flowing through R_1 and D_1 as a function of V_{in} for the circuits of Fig. 3.76. Assume a constant-voltage diode model and $V_B = 2$ V.
- **3.29.** Plot the input/output characteristic of the circuits illustrated in Fig. 3.77 assuming a constant-voltage model.
- **3.30.** Plot the currents flowing through R_1 and D_1 as a function of V_{in} for the circuits of Fig. 3.77. Assume constant-voltage diode model.
- *3.31.** Beginning with $V_{D,on} \approx 800$ mV for each diode, determine the change in V_{out} if V_{in} changes from +2.4 V to +2.5 V for the circuits shown in Fig. 3.78.
- *3.32.** Beginning with $V_{D,on} \approx 800$ mV for each diode, calculate the change in V_{out} if I_{in} changes from 3 mA to 3.1 mA in the circuits of Fig. 3.79.
- 3.33.** In Problem 3.32, determine the change in the current flowing through the 1-k Ω resistor in each circuit.
- 3.34.** Assuming $V_{in} = V_p \sin \omega t$, plot the output waveform of the circuit depicted in Fig. 3.80 for an initial condition of +0.5 V across C_1 . Assume $V_p = 5$ V.

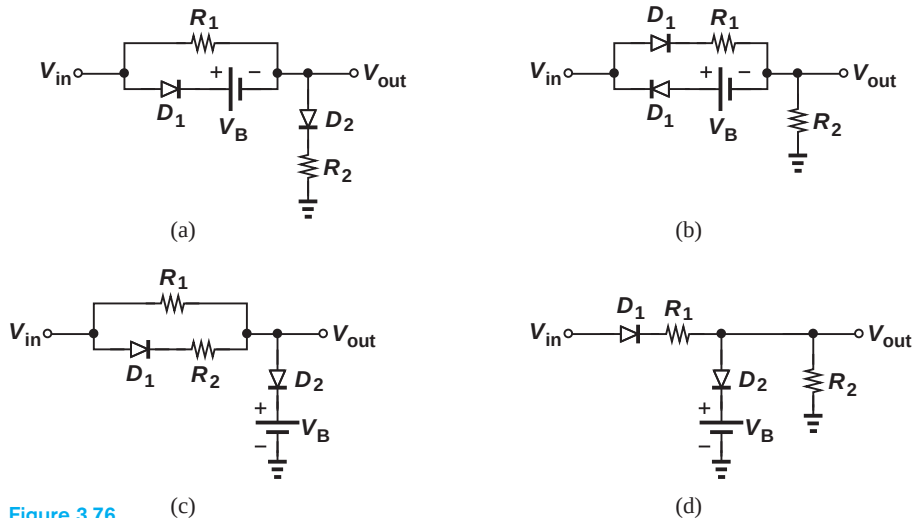


Figure 3.76

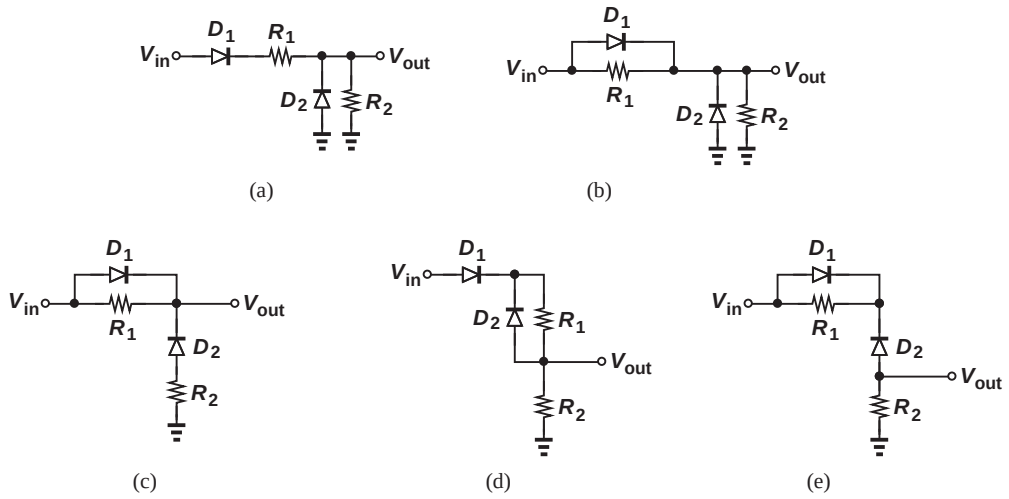


Figure 3.77

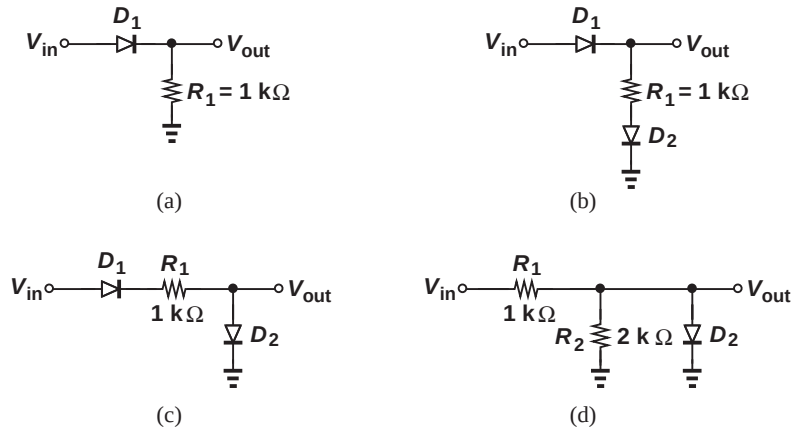


Figure 3.78

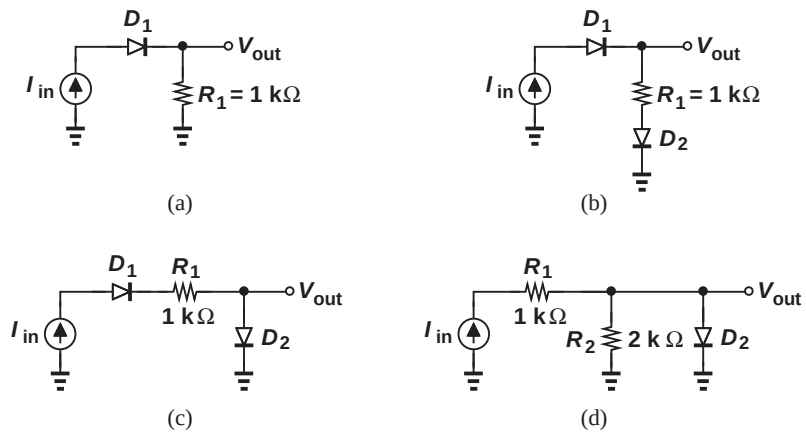


Figure 3.79

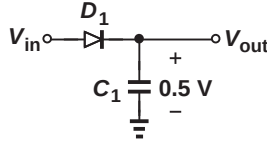


Figure 3.80

- 3.35.** Repeat Problem 3.34 for the circuit shown in Fig. 3.81.

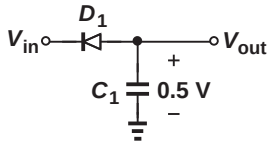


Figure 3.81

Section 3.5 Applications of Diodes

- 3.36.** Suppose the rectifier of Fig. 3.32 drives a $100\text{-}\Omega$ load with a peak voltage of 3.5 V . For a $1000\text{-}\mu\text{F}$ smoothing capacitor, calculate the ripple amplitude if the frequency is 60 Hz .
- 3.37.** A 3-V adaptor using a half-wave rectifier must supply a current of 0.5 A with a maximum ripple of 300 mV . For a frequency of 60 Hz , compute the minimum required smoothing capacitor.
- *3.38.** While constructing a full-wave rectifier, a student mistakenly has swapped the terminals of D_3 as depicted in Fig. 3.82. Explain what happens.

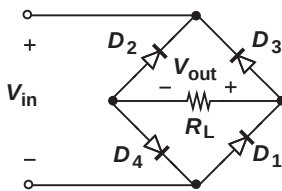


Figure 3.82

- 3.39.** Plot the voltage across each diode in Fig. 3.38(b) as a function of time if $V_{in} = V_0 \cos \omega t$. Assume a constant-voltage diode model and $V_D > V_{D,on}$.

- 3.40.** Assume the input and output grounds in a full-wave rectifier are shorted together. Draw the output waveform with and without the load capacitor and explain why the circuit does not operate as a rectifier.

- 3.41.** A full-wave rectifier is driven by a sinusoidal input $V_{in} = V_0 \cos \omega t$, where $V_0 = 3\text{ V}$ and $\omega = 2\pi(60\text{ Hz})$. Assuming $V_{D,on} = 800\text{ mV}$, determine the ripple amplitude with a $1000\text{-}\mu\text{F}$ smoothing capacitor and a load resistance of $30\text{ }\Omega$.

- 3.42.** Suppose the negative terminals of V_{in} and V_{out} in Fig. 3.38(b) are shorted together. Plot the input-output characteristic assuming an ideal diode model and explaining why the circuit does not operate as a full-wave rectifier.

- 3.43.** Suppose in Fig. 3.43, the diodes carry a current of 5 mA and the load, a current of 20 mA . If the load current increases to 21 mA , what is the change in the total voltage across the three diodes? Assume R_1 is much greater than $3r_d$.

- 3.44.** In this problem, we estimate the ripple seen by the load in Fig. 3.43 so as to appreciate the regulation provided by the diodes. For simplicity, neglect the load. Also, $f_{in} = 60\text{ Hz}$, $C_1 = 100\text{ }\mu\text{F}$, $R_1 = 1000\text{ }\Omega$, and the peak voltage produced by the transformer is equal to 5 V .

- Assuming R_1 carries a relatively constant current and $V_{D,on} \approx 800\text{ mV}$, estimate the ripple amplitude across C_1 .
- Using the small-signal model of the diodes, determine the ripple amplitude across the load.

3.45. Design the limiting circuit of Fig. 3.51 for a negative threshold of -1.9 V and a positive threshold of $+2.2\text{ V}$. Assume the input peak voltage is equal to 5 V , the maximum allowable current through each diode is 2 mA , and $V_{D,on} \approx 800\text{ mV}$.

***3.46.** In the limiting circuit of Fig. 3.51, plot the currents flowing through D_1 and D_2 as a function of time if the input is given by $V_0 \cos \omega t$ and $V_0 > V_{D,on} + V_{B1}$ and $-V_0 > -V_{D,on} - V_{B2}$.

3.47. We wish to design a circuit that exhibits the input/output characteristic shown in Fig. 3.83. Using $1\text{-k}\Omega$ resistors, ideal diodes, and other components, construct the circuit.

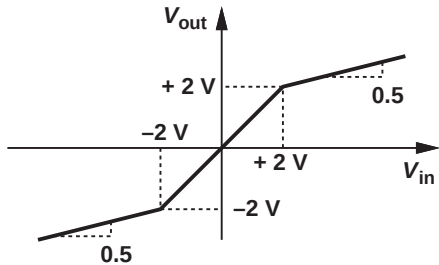


Figure 3.83

***3.48.** “Wave-shaping” applications require the input/output characteristic illustrated in Fig. 3.84. Using ideal diodes and other components, construct a circuit that provides such a characteristic. (The value of resistors is not unique.)

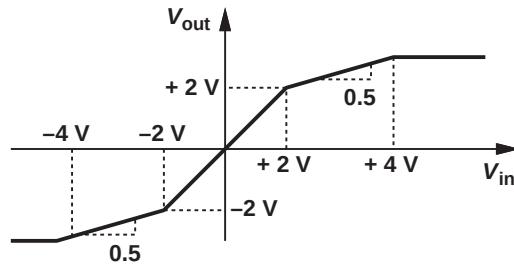


Figure 3.84

****3.49.** Suppose a triangular waveform is applied to the characteristic of Fig. 3.84 as shown in Fig. 3.85. Plot the output waveform and note that it is a rough approximation of a sinusoid. How should the input-output characteristic be modified so that the output becomes a better approximation of a sinusoid?

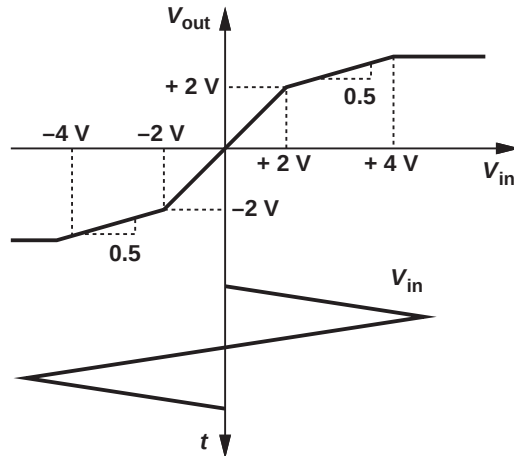


Figure 3.85

SPICE PROBLEMS

In the following problems, assume $I_S = 5 \times 10^{-16}\text{ A}$.

3.50. The half-wave rectifier of Fig. 3.86 must deliver a current of 5 mA to R_1 for a peak input level of 2 V .

(a) Using hand calculations, determine the required value of R_1 .

(b) Verify the result by SPICE.

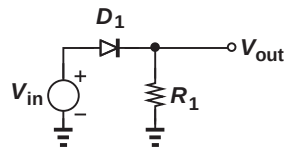


Figure 3.86

- 3.51.** In the circuit of Fig. 3.87, $R_1 = 500\ \Omega$ and $R_2 = 1\ \text{k}\Omega$. Use SPICE to construct the input/output characteristic for $-2\ \text{V} < V_{in} < +2\ \text{V}$. Also, plot the current flowing through R_1 as a function of V_{in} .

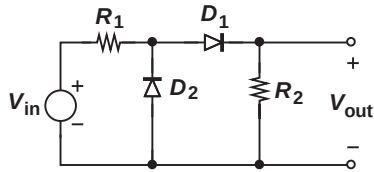


Figure 3.87

- 3.52.** The rectifier shown in Fig. 3.88 is driven by a 60-Hz sinusoid input with a peak amplitude of 5 V. Using the transient analysis in SPICE,
- Determine the peak-to-peak ripple at the output.
 - Determine the peak current flowing through D_1 .
 - Compute the heaviest load (smallest R_L) that the circuit can drive while maintaining a ripple less than $200\ \text{mV}_{pp}$.

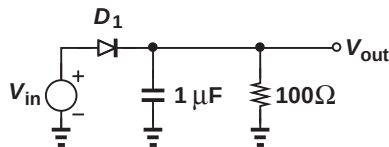


Figure 3.88

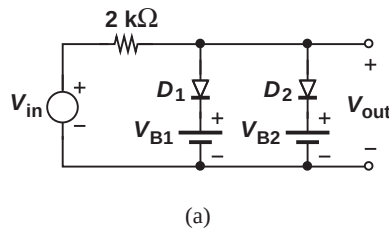


Figure 3.90

- 3.53.** The circuit of Fig. 3.89 is used in some analog circuits. Plot the input/output characteristic for $-2\ \text{V} < V_{in} < +2\ \text{V}$ and determine the maximum input range across which $|V_{in} - V_{out}| < 5\ \text{mV}$.

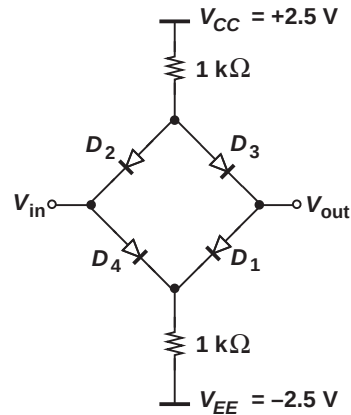
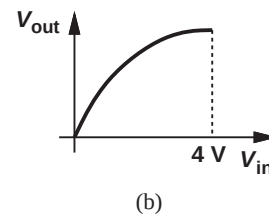


Figure 3.89

- 3.54.** The circuit shown in Fig. 3.90 can provide an approximation of a sinusoid at the output in response to a triangular input waveform. Using the dc analysis in SPICE to plot the input/output characteristic for $0 < V_{in} < 4\ \text{V}$, determine the values of V_{B1} and V_{B2} such that the characteristic closely resembles a sinusoid.



Physics of Bipolar Transistors

PROBLEMS

In the following problems, unless otherwise stated, assume the bipolar transistors operate in the active mode.

Section 4.1 General Considerations

- 4.1. Suppose the voltage-dependent current source of Fig. 4.1(a) is constructed with $K = 20 \text{ mA/V}$. What value of load resistance in Fig. 4.1(b) is necessary to achieve a voltage gain of 15?
- 4.2. A resistance of R_S is placed in series with the input voltage source in Fig. 4.2. Determine V_{out}/V_{in} .
- 4.3. Repeat Problem 4.2 but assuming that r_{in} and K are related: $r_{in} = a/x$ and $K = bx$. Plot the voltage gain as a function of x .

Section 4.3 Operation of Bipolar Transistor in Active Mode

- 4.4. Due to a manufacturing error, the base width of a bipolar transistor has increased by a factor of two. How does the collector current change?
- 4.5. In the circuit of Fig. 4.48, $I_{S1} = I_{S2} = 3 \times 10^{-16} \text{ A}$.
 - (a) Calculate V_B such that $I_X = 1 \text{ mA}$.
 - (b) With the value of V_B found in (a), choose I_{S3} such that $I_Y = 2.5 \text{ mA}$.
- 4.6. In the circuit of Fig. 4.49, it is observed that the collector currents of Q_1 and Q_2 are equal if $V_{BE1} - V_{BE2} = 20 \text{ mV}$. Determine the ratio of transistor cross section areas if the other device parameters are identical.

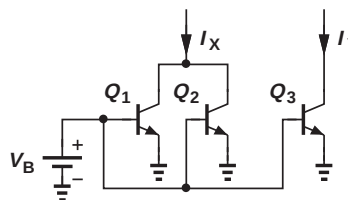


Figure 4.48

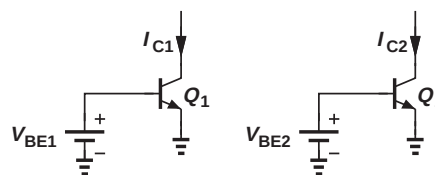


Figure 4.49

4.7. Consider the circuit shown in Fig. 4.50.

- (a) If $I_{S1} = 2I_{S2} = 5 \times 10^{-16}$ A, determine V_B such that $I_X = 1.2$ mA.
 (b) What value of R_C places the transistors at the edge of the active mode?

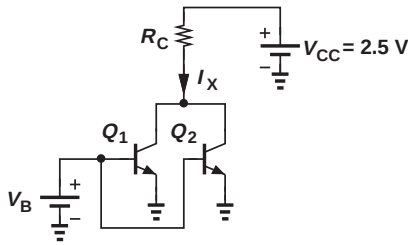


Figure 4.50

4.8. Repeat Problem 4.7 if V_{CC} is lowered to 1.5 V.

4.9. Calculate V_X in Fig. 4.51 if $I_S = 6 \times 10^{-16}$ A.

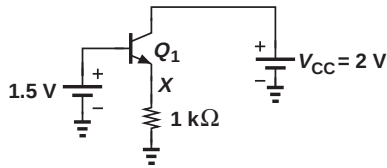


Figure 4.51

4.10. In the circuit of Fig. 4.52, determine the maximum value of V_{CC} that places Q_1 at the edge of saturation. Assume $I_S = 3 \times 10^{-16}$ A.

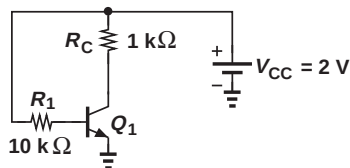


Figure 4.52

4.11. Consider the circuit shown in Fig. 4.53. Calculate the value of V_B that places Q_1 at the edge of the active region. Assume $I_S = 5 \times 10^{-16}$ A.

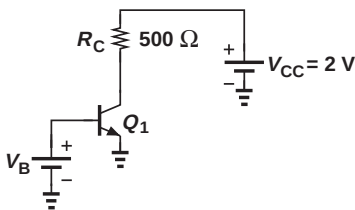


Figure 4.53

4.12. An integrated circuit requires two current sources: $I_1 = 1$ mA and $I_2 = 1.5$ mA. Assuming that only integer multiples of a unit bipolar transistor having $I_S = 3 \times 10^{-16}$ A can be placed in parallel, and only a single voltage source, V_B , is available (Fig. 4.54), construct the required circuit with minimum number of unit transistors.

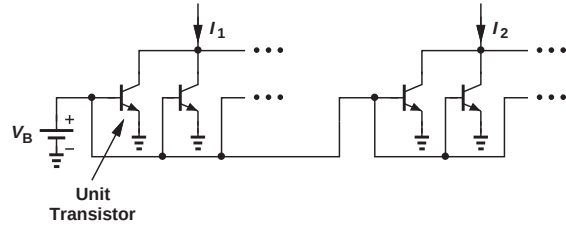


Figure 4.54

4.13. Repeat Problem 4.12 for three current sources $I_1 = 0.2$ mA, $I_2 = 0.3$ mA, and $I_3 = 0.45$ mA.

4.14. Consider the circuit shown in Fig. 4.55, assuming $\beta = 100$ and $I_S = 7 \times 10^{-16}$ A. If $R_1 = 10$ kΩ, determine V_B such that $I_C = 1$ mA.

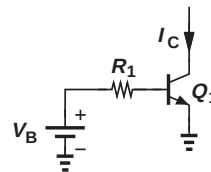


Figure 4.55

4.15. In the circuit of Fig. 4.55, $V_B = 800$ mV and $R_B = 10$ kΩ. Calculate the collector current.

4.16. In the circuit depicted in Fig. 4.56, $I_{S1} = 2I_{S2} = 4 \times 10^{-16}$ A. If $\beta_1 = \beta_2 = 100$ and $R_1 = 5$ kΩ, compute V_B such that $I_X = 1$ mA.

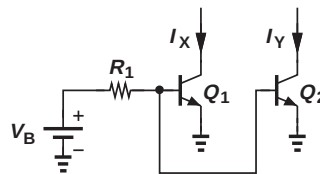


Figure 4.56

4.17. In the circuit of Fig. 4.56, $I_{S1} = 3 \times 10^{-16}$ A, $I_{S2} = 5 \times 10^{-16}$ A, $\beta_1 = \beta_2 = 100$, $R_1 = 5 \text{ k}\Omega$, and $V_B = 800 \text{ mV}$. Calculate I_X and I_Y .

4.18. The base-emitter junction of a transistor is driven by a constant voltage. Suppose a voltage source is applied between the base and collector. If the device operates in the forward active region, prove that a change in base-collector voltage results in no change in the collector and base currents. (Neglect the Early effect.)

Section 4.4 Bipolar Transistor Models and Characteristics

4.19. Most applications require that the transconductance of a transistor remain relatively constant as the signal level varies. Of course, since the signal changes the collector current, $g_m = I_C/V_T$, does vary. Nonetheless, proper design ensures negligible variation, e.g., $\pm 10\%$. If a bipolar device is biased at $I_C = 1 \text{ mA}$, what is the largest change in V_{BE} that guarantees only $\pm 10\%$ variation in g_m ?

4.20. A transistor with $I_S = 6 \times 10^{-16}$ A must provide a transconductance of $1/(13 \Omega)$. What base-emitter voltage is required?

4.21. Determine the operating point and the small-signal model of Q_1 for each of the circuits shown in Fig. 4.57. Assume $I_S = 8 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

4.22. Determine the operating point and the small-signal model of Q_1 for each of the circuits shown in Fig. 4.58. Assume $I_S = 8 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

4.23. A fictitious bipolar transistor exhibits an I_C - V_{BE} characteristic given by

$$I_C = I_S \exp \frac{V_{BE}}{nV_T}, \quad (4.119)$$

where n is a constant coefficient. Construct the small-signal model of the device if I_C is still equal to βI_B .

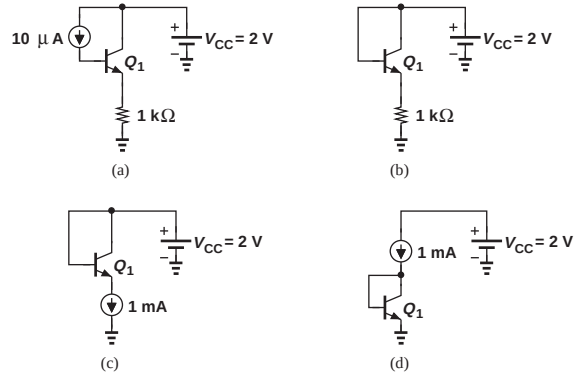


Figure 4.58

***4.24.** A fictitious bipolar transistor exhibits the following relationship between its base and collector currents:

$$I_C = aI_B^2, \quad (4.120)$$

where a is a constant coefficient. Construct the small-signal model of the device if I_C is still equal to $I_S \exp(V_{BE}/V_T)$.

4.25. The collector voltage of a bipolar transistor varies from 1 V to 3 V while the base-emitter voltage remains constant. What Early voltage is necessary to ensure that the collector current changes by less than 5%?

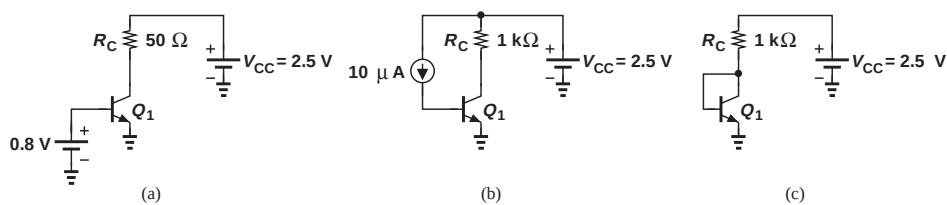


Figure 4.57

- *4.26. In the circuit of Fig. 4.59, $I_S = 5 \times 10^{-17}$ A. Determine V_X for (a) $V_A = \infty$, and (b) $V_A = 5$ V.

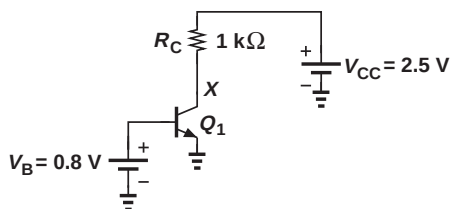


Figure 4.59

- 4.27. In the circuit of Fig. 4.60, V_{CC} changes from 2.5 to 3 V. Assuming $I_S = 1 \times 10^{-17}$ A and $V_A = 5$ V, determine the change in the collector current of Q_1 .
- 4.28. In Problem 4.27, we wish to decrease V_B to compensate for the change in I_C . Determine the new value of V_B .

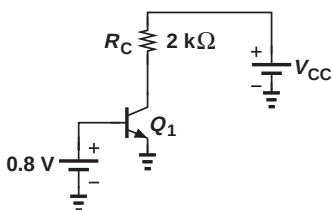


Figure 4.60

- 4.29. In the circuit of Fig. 4.61, n identical transistors are placed in parallel. If $I_S = 5 \times 10^{-16}$ A and $V_A = 8$ V for each device, construct the small-signal model of the equivalent transistor.

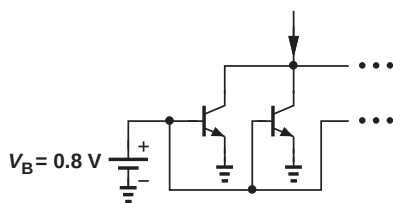


Figure 4.61

- 4.30. A bipolar current source is designed for an output current of 2 mA. What value of V_A guarantees an output resistance greater than 10 kΩ?

- *4.31. Consider the circuit shown in Fig. 4.62, where I_1 is a 1-mA ideal current source and $I_S = 3 \times 10^{-17}$ A.

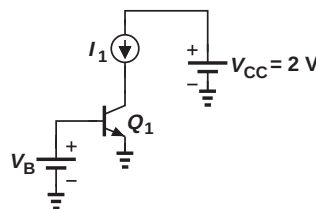


Figure 4.62

- (a) Assuming $V_A = \infty$, determine V_B such that $I_C = 1$ mA.
- (b) If $V_A = 5$ V, determine V_B such that $I_C = 1$ mA for a collector-emitter voltage of 1.5 V.

- 4.32. Consider the circuit shown in Fig. 4.63, where $I_S = 6 \times 10^{-16}$ A and $V_A = \infty$.

- (a) Determine V_B such that Q_1 operates at the edge of the active region.
- (b) If we allow soft saturation, e.g., a collector-base forward bias of 200 mV, by how much can V_B increase?

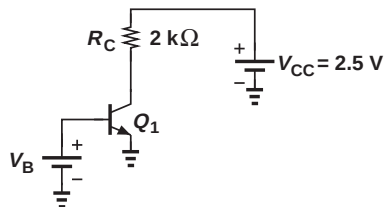


Figure 4.63

- 4.33. For the circuit depicted in Fig. 4.64, calculate the maximum value of V_{CC} that produces a collector-base forward bias of 200 mV. Assume $I_S = 7 \times 10^{-16}$ A and $V_A = \infty$.

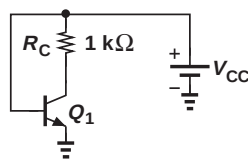


Figure 4.64

- 4.34.** Consider the circuit shown in Fig. 4.65, where $I_S = 5 \times 10^{-16}$ A and $V_A = \infty$. If V_B is chosen to forward-bias the base-collector junction by 200 mV, what is the collector current?

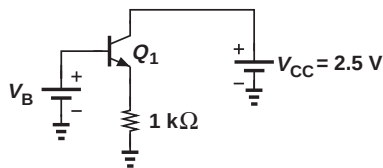


Figure 4.65

- *4.35.** Assume $I_S = 2 \times 10^{-17}$ A, $V_A = \infty$, and $\beta = 100$ in Fig. 4.66. What is the maximum value of R_C if the collector-base must experience a forward bias of less than 200 mV?

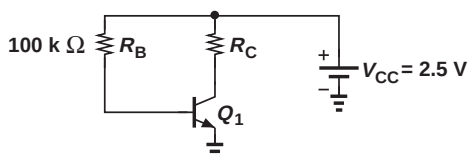


Figure 4.66

- 4.36.** In the circuit of Fig. 4.67, $\beta = 100$ and $V_A = \infty$. Calculate the value of I_S such that the base-collector junction is forward-biased by 200 mV.

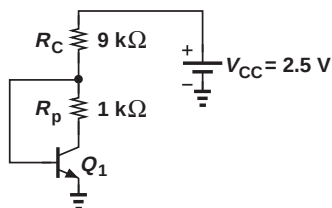


Figure 4.67

Section 4.6 pnp Transistor

- 4.37.** If $I_{S1} = 3I_{S2} = 6 \times 10^{-16}$ A, calculate I_X in Fig. 4.68.

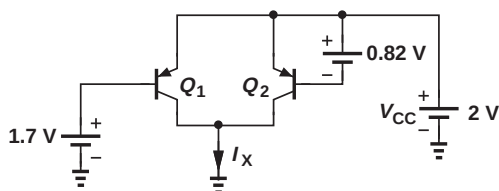


Figure 4.68

- 4.38.** In the circuit of Fig. 4.69, it is observed that $I_C = 3$ mA. If $\beta = 100$, calculate I_S .

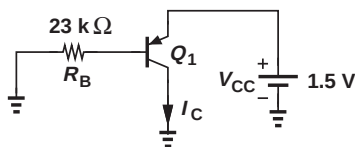


Figure 4.69

- 4.39.** Determine the collector current of Q_1 in Fig. 4.70 if $I_S = 2 \times 10^{-17}$ A and $\beta = 100$.

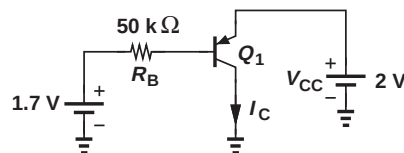


Figure 4.70

- 4.40.** Determine the value of I_S in Fig. 4.71 such that Q_1 operates at the edge of the active mode.

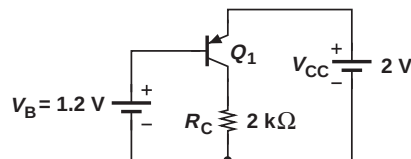


Figure 4.71

- 4.41.** What is the value of β that places Q_1 at the edge of the active mode in Fig. 4.72? Assume $I_S = 8 \times 10^{-16}$ A.

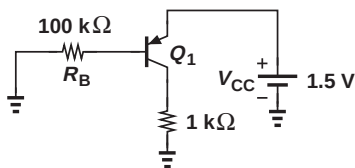


Figure 4.72

- 4.42.** Calculate the collector current of Q_1 in Fig. 4.73 if $I_S = 3 \times 10^{-17}$ A.

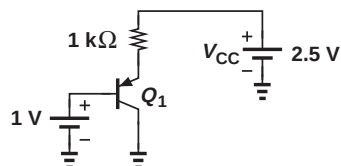


Figure 4.73

- *4.43.** Determine the operating point and the small-signal model of Q_1 for each of the circuits shown in Fig. 4.74. Assume $I_S = 3 \times 10^{-17}$ A, $\beta = 100$, and $V_A = \infty$.

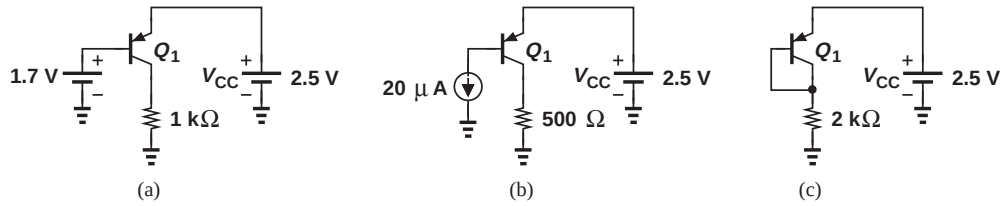


Figure 4.74

- 4.44.** In the circuit of Fig. 4.75, $I_S = 5 \times 10^{-17}$ A. Calculate V_X for (a) $V_A = \infty$, and (b) $V_A = 6$ V.

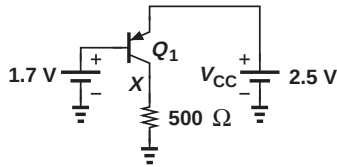


Figure 4.75

- *4.45.** Determine the operating point and the small-signal model of Q_1 for each of the circuits shown in Fig. 4.76. Assume $I_S = 3 \times 10^{-17}$ A, $\beta = 100$, and $V_A = \infty$.

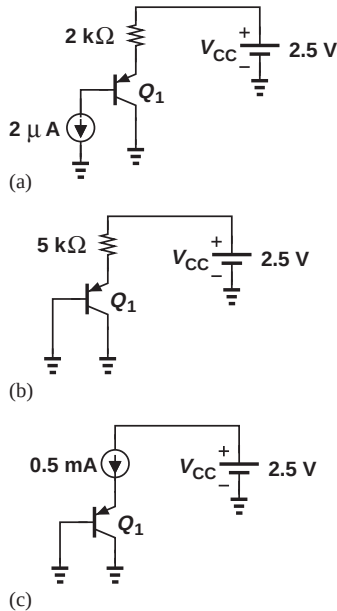


Figure 4.76

- 4.46.** A *pnp* current source must provide an output current of 2 mA with an output resis-

tance of 60 kΩ. What is the required Early voltage?

- 4.47.** Repeat Problem 4.46 for a current of 1 mA and compare the results.

- *4.48.** Suppose $V_A = 5$ V in the circuit of Fig. 4.77.

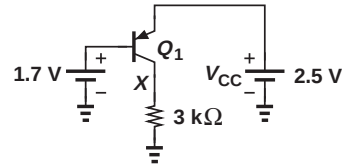


Figure 4.77

- (a) What value of I_S places Q_1 at the edge of the active mode?
(b) How does the result in (a) change if $V_A = \infty$?

- *4.49.** Consider the circuit depicted in Fig. 4.78, where $I_S = 6 \times 10^{-16}$ A, $V_A = 5$ V, and $I_1 = 2$ mA.

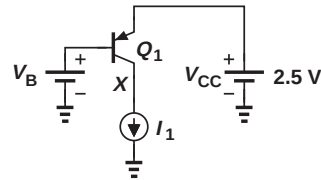


Figure 4.78

- (a) What value of V_B yields $V_X = 1$ V?
(b) If V_B changes from the value found in (a) by 0.1 mV, what is the change in V_X ?
(c) Construct the small-signal model of the transistor.

- *4.50.** The terminal currents in the small-signal model of Fig. 4.43 do not seem to agree with those in the large-signal model of Fig. 4.40. Explain why this is not an inconsistency.

4.51. In the circuit of Fig. 4.79, $\beta = 100$ and $V_A = \infty$.

- Determine I_S such that Q_1 experiences a collector-base forward bias of 200 mV.
- Calculate the transconductance of the transistor.

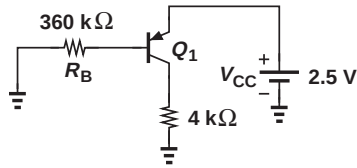


Figure 4.79

****4.52.** Determine the region of operation of Q_1 in each of the circuits shown in Fig. 4.80.

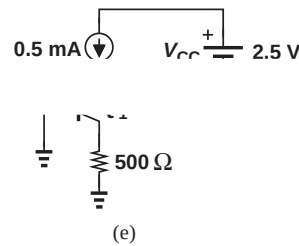
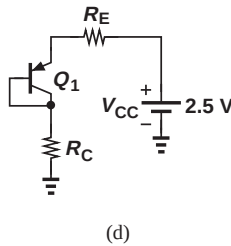
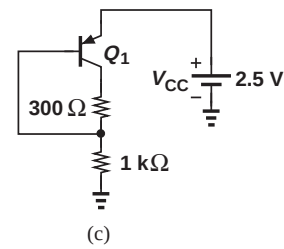
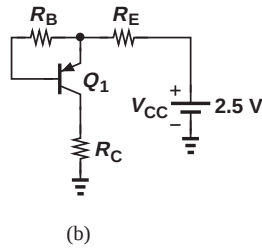
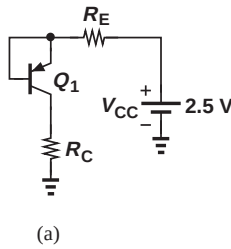


Figure 4.80

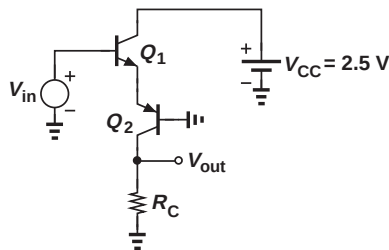


Figure 4.81

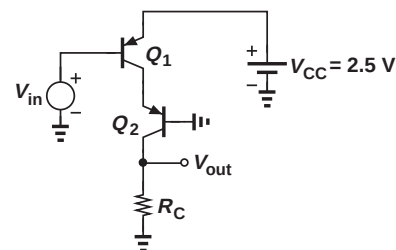


Figure 4.82

Assume $I_S = 5 \times 10^{-16}$ A, $\beta = 100$, $V_A = \infty$.

****4.53.** Consider the circuit shown in Fig. 4.81, where $I_{S1} = 3I_{S2} = 5 \times 10^{-16}$ A, $\beta_1 = 100$, $\beta_2 = 50$, $V_A = \infty$, and $R_C = 500 \Omega$.

- We wish to forward-bias the collector-base junction of Q_2 by no more than 200 mV. What is the maximum allowable value of V_{in} ?
- With the value found in (a), calculate the small-signal parameters of Q_1 and Q_2 and construct the equivalent circuit.

****4.54.** Repeat Problem 4.53 for the circuit depicted in Fig. 4.82 but for part (a), determine the minimum allowable value of V_{in} . Verify that Q_1 operates in the active mode.

- **4.55.** Repeat Problem 4.53 for the circuit illustrated in Fig. 4.83.

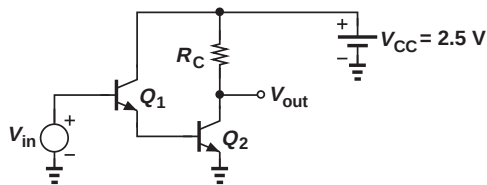


Figure 4.83

- **4.56.** In the circuit of Fig. 4.84,
 $I_{S1} = 2I_{S2} = 6 \times 10^{-17} \text{ A}$,
 $\beta_1 = 80$ and $\beta_2 = 100$.

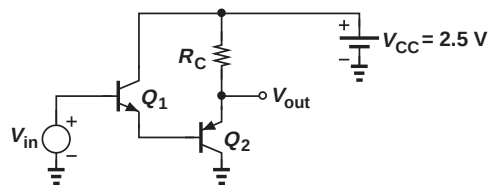


Figure 4.84

- What value of V_{in} yields a collector current of 2 mA for Q_2 ?
- With the value found in (a), calculate the small-signal parameters of Q_1 and Q_2 and construct the equivalent circuit.

SPICE PROBLEMS

In the following problems, assume $I_{S,npn} = 5 \times 10^{-16} \text{ A}$, $\beta_{npn} = 100$, $V_{A,npn} = 5 \text{ V}$, $I_{S,pnp} = 8 \times 10^{-16} \text{ A}$, $\beta_{pnp} = 50$, $V_{A,pnp} = 3.5 \text{ V}$.

- 4.57.** Plot the input/output characteristic of the circuit shown in Fig. 4.85 for $0 < V_{in} < 2.5 \text{ V}$. What value of V_{in} places the transistor at the edge of saturation?

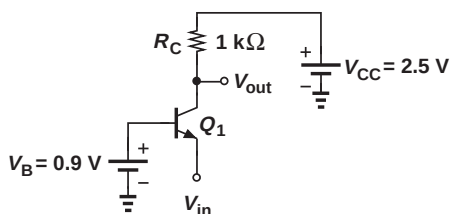


Figure 4.85

- 4.58.** Repeat Problem 4.57 for the stage depicted in Fig. 4.86. At what value of V_{in} does Q_1 carry a collector current of 1 mA?

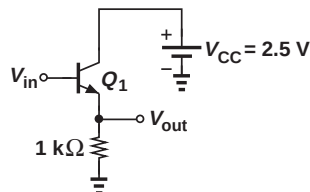


Figure 4.86

- 4.59.** Plot I_{C1} and I_{C2} as a function of V_{in} for the circuits shown in Fig. 4.87

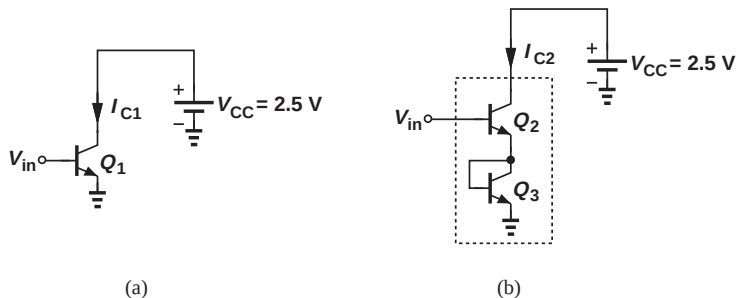


Figure 4.87

- 4.60.** Plot the input/output characteristic of the circuit illustrated in Fig. 4.88 for $0 < V_{in} < 2\text{ V}$. What value of V_{in} yields a transconductance of $(50\ \Omega)^{-1}$ for Q_1 ?

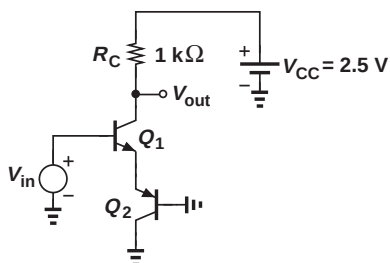


Figure 4.88

- 4.61.** Plot the input/output characteristic of the stage shown in Fig. 4.89 for $0 < V_{in} < 2.5\text{ V}$. At what value of V_{in} do Q_1 and Q_2 carry equal collector currents? Can you explain this result intuitively?

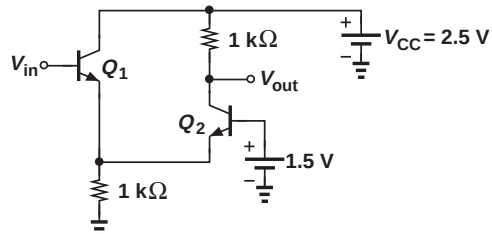
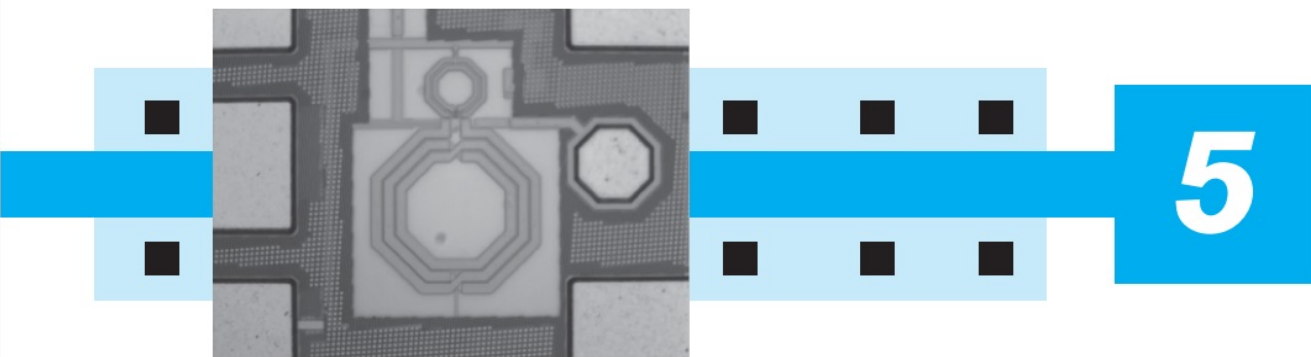


Figure 4.89



Bipolar Amplifiers

PROBLEMS

Section 5.1.1 Input and Output Impedances

- 5.1.** An antenna can be modeled as a Thevenin equivalent having a sinusoidal voltage source $V_0 \cos \omega t$ and an output resistance R_{out} . Determine the average power delivered to a load resistance R_L and plot the result as a function of R_L .
- 5.2.** Determine the small-signal input resistance of the circuits shown in Fig. 5.104. Assume all diodes are forward-biased. (Recall from Chapter 3 that each diode behaves as a linear resistance if the voltage and current changes are small.)

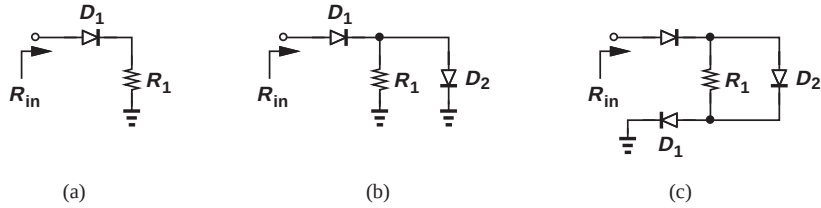


Figure 5.104

5.3. Compute the input resistance of the circuits depicted in Fig. 5.105. Assume $V_A = \infty$.

5.4. Compute the output resistance of the circuits depicted in Fig. 5.106.

5.5. Determine the input impedance of the circuits depicted in Fig. 5.107. Assume $V_A = \infty$.

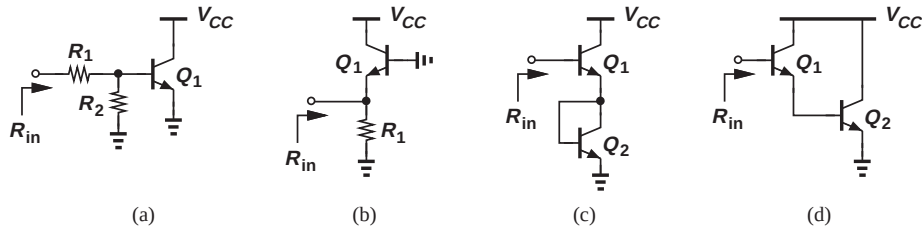


Figure 5.105

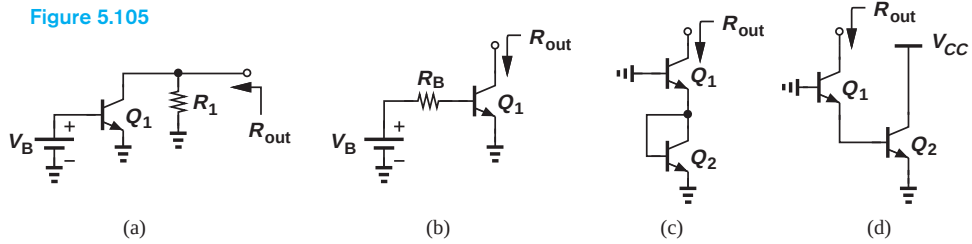


Figure 5.106

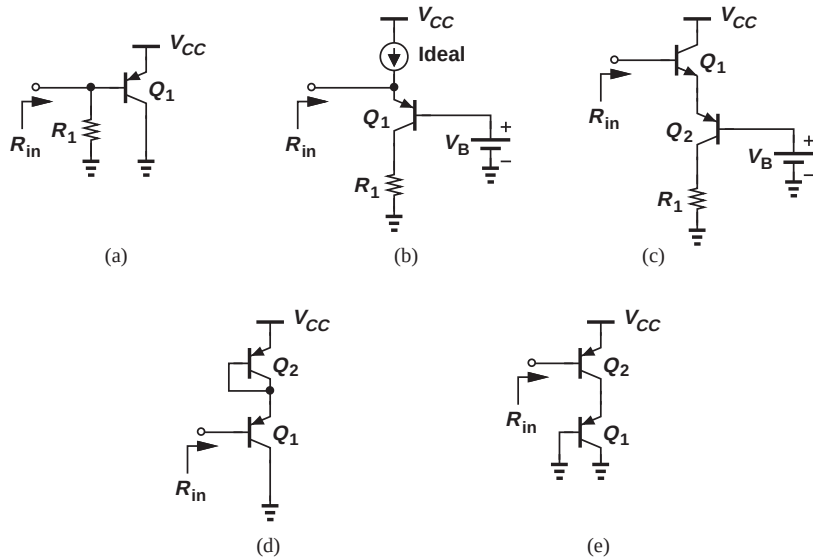


Figure 5.107

5.6. Compute the output impedance of the circuits shown in Fig. 5.108.

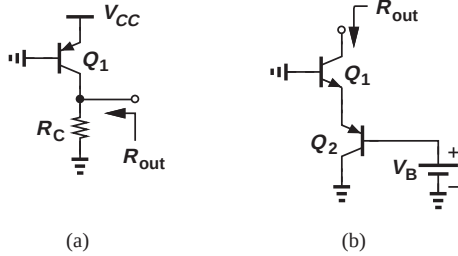


Figure 5.108

Sections 5.2.1 and 5.2.2 Simple and Resistive Divider Biasing

5.7. Compute the bias point of the circuits depicted in Fig. 5.109. Assume $\beta = 100$, $I_S = 6 \times 10^{-16}$ A, and $V_A = \infty$.

5.8. Construct the small-signal equivalent of each of the circuits in Problem 5.7.

***5.9.** Calculate the bias point of the circuits shown in Fig. 5.110. Assume $\beta = 100$, $I_S = 5 \times 10^{-16}$ A, and $V_A = \infty$.

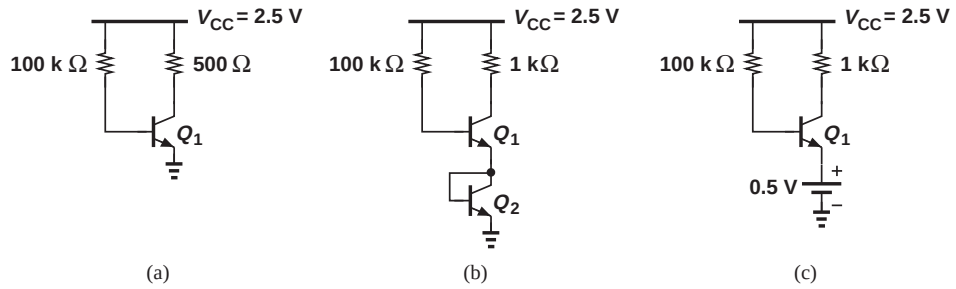


Figure 5.109

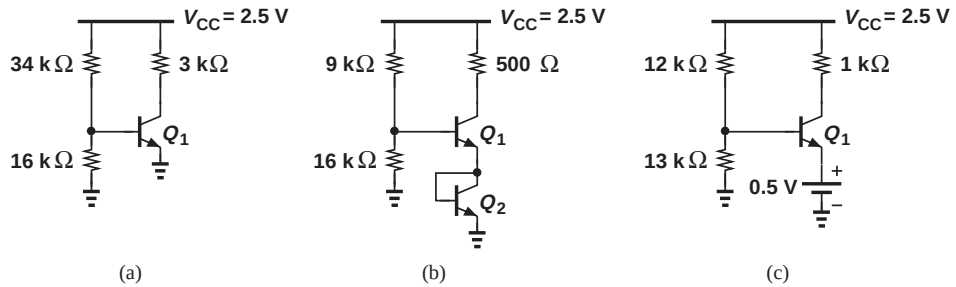


Figure 5.110

5.10. Construct the small-signal equivalent of each of the circuits in Problem 5.9.

5.11. In the circuit of Fig. 5.111, $\beta = 100$ and $V_A = \infty$.

(a) If the collector current of Q_1 is equal to 0.5 mA, calculate the value of I_S .

(b) If Q_1 is biased at the edge of saturation, calculate the value of I_S .

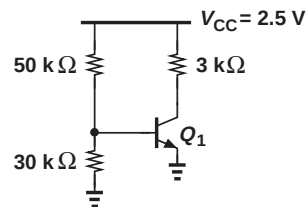


Figure 5.111

5.12. Consider the circuit shown in Fig. 5.112, where $\beta = 100$, $I_S = 6 \times 10^{-16}$ A, and $V_A = \infty$.

- What is the minimum value of R_B that guarantees operation in the active mode?
- With the value found in R_B , how much base-collector forward bias is sustained if β rises to 200?

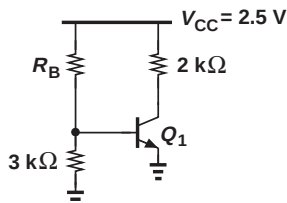


Figure 5.112

5.13. The circuit of Fig. 5.113 must be designed for an input impedance of greater than $10 \text{ k}\Omega$ and a g_m of at least $1/(260 \Omega)$. If $\beta = 100$, $I_S = 2 \times 10^{-17}$ A, and $V_A = \infty$, determine the minimum allowable values of R_1 and R_2 .

***5.14.** Repeat Problem 5.13 for a g_m of at least $1/(26 \Omega)$. Explain why no solution exists.

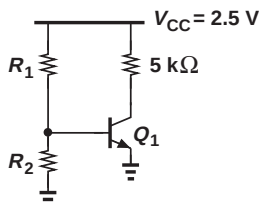


Figure 5.113

***5.15.** We wish to design the CE stage depicted in Fig. 5.114 for a gain ($= g_m R_C$) of A_0 with an output impedance of R_0 . What is the maximum achievable input impedance here? Assume $V_A = \infty$.

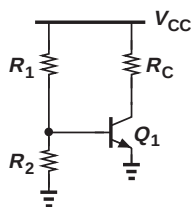


Figure 5.114

Section 5.2.3 Biasing with Emitter Degeneration

5.16. The circuit of Fig. 5.115 is designed for a collector current of 0.25 mA . Assume $I_S = 6 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

- Determine the required value of R_1 .
- What is the error in I_C if R_E deviates from its nominal value by 5%?

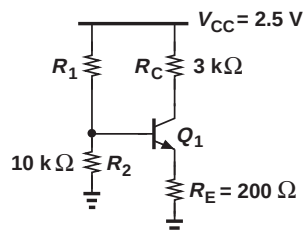


Figure 5.115

5.17. In the circuit of Fig. 5.116, determine the maximum value of R_2 that guarantees operation of Q_1 in the active mode. Assume $\beta = 100$, $I_S = 10^{-17}$ A, and $V_A = \infty$.

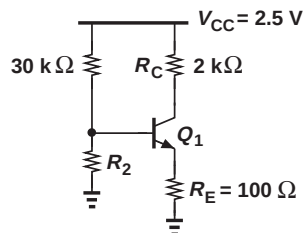


Figure 5.116

5.18. In the circuit depicted in Fig. 5.117, $I_{S1} = I_{S2} = 4 \times 10^{-16}$ A, $\beta_1 = \beta_2 = 100$, and $V_A = \infty$.

- Determine the operating point of the transistor.
- Draw the small-signal equivalent circuit.

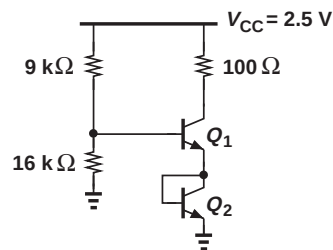


Figure 5.117

***5.19.** Consider the circuit shown in Fig. 5.118, where $I_{S1} = 2I_{S2} = 5 \times 10^{-16}$ A, $\beta_1 = \beta_2 = 100$, and $V_A = \infty$.

(a) Determine the collector currents of Q_1 and Q_2 .

(b) Construct the small-signal equivalent circuit.

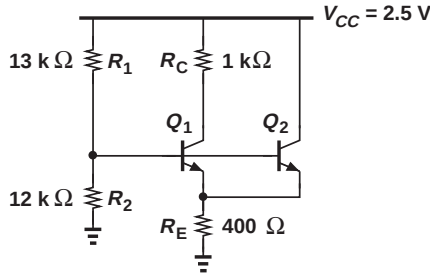


Figure 5.118

Section 5.2.4 Self-Biased Stage

5.20. The circuit of Fig. 5.119 must be biased with a collector current of 1 mA. Compute the required value of R_B if $I_S = 3 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

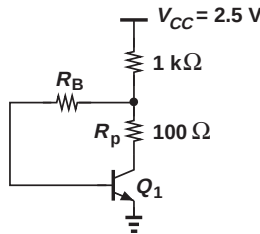


Figure 5.119

5.21. In the circuit of Fig. 5.120, $V_X = 1.1$ V. If $\beta = 100$ and $V_A = \infty$, what is the value of I_S ?

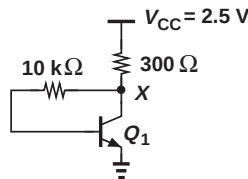


Figure 5.120

5.22. Due to a manufacturing error, a parasitic resistor, R_P , has appeared in series with

the collector of Q_1 in Fig. 5.121. What is the minimum allowable value of R_B if the base-collector forward bias must not exceed 200 mV? Assume $I_S = 3 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

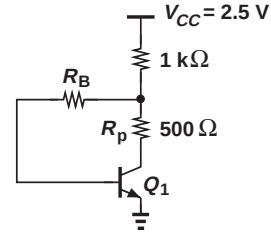


Figure 5.121

5.23. Consider the circuit shown in Fig. 5.122, where $I_S = 6 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$. Calculate the operating point of Q_1 .

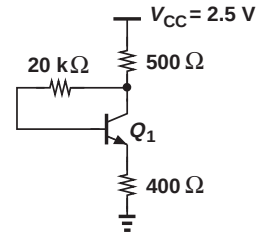


Figure 5.122

***5.24.** In the circuit of Fig. 5.123, $I_S = 8 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

(a) Determine the operating point of Q_1 .
(b) Draw the small-signal equivalent circuit.

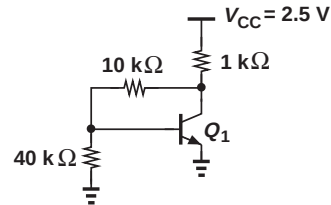


Figure 5.123

****5.25.** In the circuit of Fig. 5.124, $I_{S1} = I_{S2} = 3 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

(a) Calculate V_B such that Q_1 carries a collector current of 1 mA.
(b) Construct the small-signal equivalent circuit.

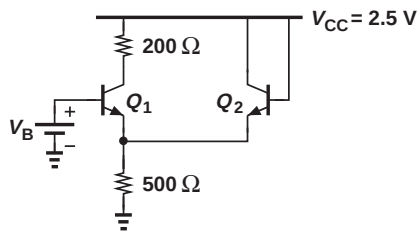


Figure 5.124

Section 5.2.5 Biasing of npn Transistors

5.26. Determine the bias point of each circuit shown in Fig. 5.125. Assume $\beta_{npn} = 2\beta_{pnp} = 100$, $I_S = 9 \times 10^{-16}$ A, and $V_A = \infty$.

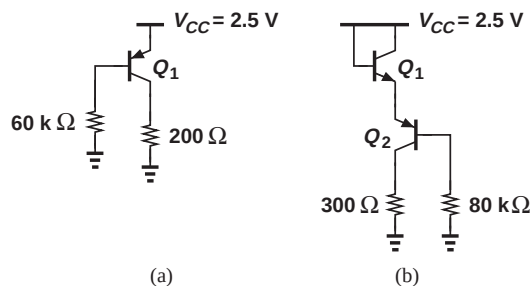


Figure 5.125

5.27. Construct the small-signal model of the circuits in Problem 5.26.

5.28. Calculate the bias point of the circuits shown in Fig. 5.126. Assume $\beta_{npn} = 2\beta_{pnp} = 100$, $I_S = 9 \times 10^{-16}$ A, and $V_A = \infty$.

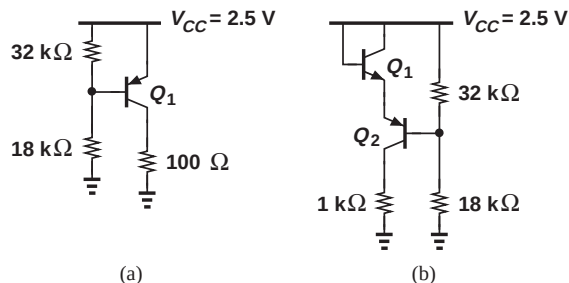


Figure 5.126

5.29. Draw the small-signal model of the circuits in Problem 5.28.

5.30. Calculate the value of R_E in Fig. 5.127 such that Q_1 sustains a reverse bias of 300 mV across its base-collector junction. Assume

$\beta = 50$, $I_S = 8 \times 10^{-16}$ A, and $V_A = \infty$. What happens if the value of R_E is halved?

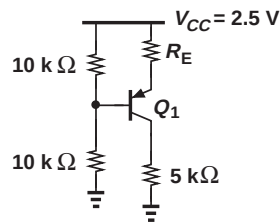


Figure 5.127

5.31. We have chosen R_B in Fig. 5.128 to place Q_1 at the edge of saturation. But the actual value of this resistor can vary by $\pm 5\%$. Determine the forward- or reverse-bias across the base-collector junction at these two extremes. Assume $\beta = 50$, $I_S = 8 \times 10^{-16}$ A, and $V_A = \infty$.

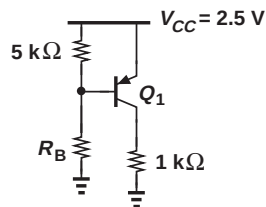


Figure 5.128

5.32. If $\beta = 80$ and $V_A = \infty$, what value of I_S yields a collector current of 1 mA in Fig. 5.129?

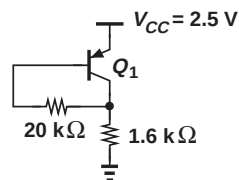


Figure 5.129

***5.33.** The topology depicted in Fig. 5.130(a) is called a “ V_{BE} multiplier.” (The npn counterpart has a similar topology.) Constructing the circuit shown in Fig. 5.130(b), determine the collector-emitter voltage of Q_1 if the base current is negligible. (The npn counterpart can also be used.)

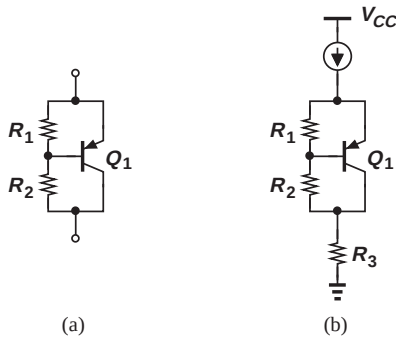


Figure 5.130

Section 5.3.1 Common-Emitter Topology

- 5.34.** We wish to design the CE stage of Fig. 5.131 for a voltage gain of 20. What is the minimum allowable supply voltage if Q_1 must remain in the active mode? Assume $V_A = \infty$ and $V_{BE} = 0.8$ V.

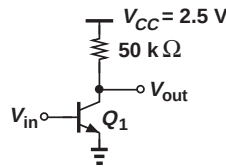


Figure 5.131

- 5.35.** The circuit of Fig. 5.132 must be designed for maximum voltage gain while maintaining Q_1 in the active mode. If $V_A = 10$ V and $V_{BE} = 0.8$ V, calculate the required bias current.

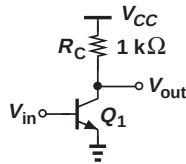


Figure 5.132

- 5.36.** Suppose the bipolar transistor in Fig. 5.133 exhibits the following hypothetical characteristic:

$$I_C = I_S \exp \frac{V_{BE}}{2V_T}, \quad (5.368)$$

and no Early effect. Compute the voltage gain for a bias current of 1 mA.

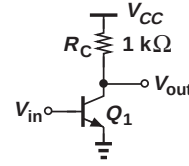


Figure 5.133

- 5.37.** The CE stage of Fig. 5.134 employs an ideal current source as the load. If the voltage gain is equal to 50 and the output impedance equal to 10 kΩ, determine the bias current of the transistor.

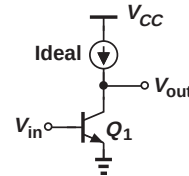


Figure 5.134

- **5.38.** Determine the voltage gain and I/O impedances of the circuits shown in Fig. 5.135. Assume $V_A = \infty$. Transistor Q_2 in Figs. 5.135(d) and (e) operates in soft saturation.

- **5.39.** Repeat Problem 5.38 with $V_A < \infty$.

- 5.40.** Consider Eq. (5.157) for the gain of a de-generated CE stage. Writing $g_m = I_C/V_T$, we note that g_m and hence the voltage gain vary if I_C changes with the signal level. For the following two cases, determine the relative change in the gain if I_C varies by 10%: (a) $g_m R_E$ is nominally equal to 3; (b) $g_m R_E$ is nominally equal to 7. The more constant gain in the second case translates to greater circuit linearity.

- 5.41.** Express the voltage gain of the stage depicted in Fig. 5.136 in terms of the collector bias current, I_C , and V_T . If $V_A = \infty$, what is the gain if the dc voltage drops across R_C and R_E are equal to $20V_T$ and $5V_T$, respectively?

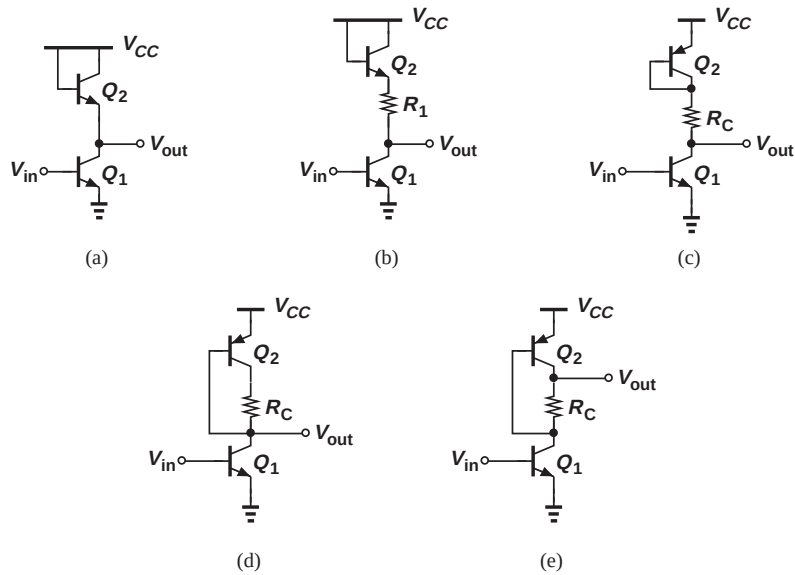


Figure 5.135

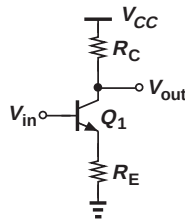


Figure 5.136

- 5.42.** We wish to design the degenerated stage of Fig. 5.137 for a voltage gain of 10 with Q_1 operating at the edge of saturation. Calculate the bias current and the value of R_C if $\beta = 100$, $I_S = 5 \times 10^{-16} \text{ A}$, and $V_A = \infty$. Calculate the input impedance of the circuit.

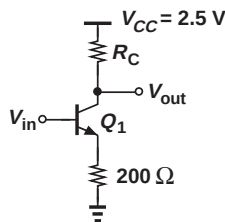


Figure 5.137

- *5.43.** Repeat Problem 5.42 for a voltage gain of 100. Explain why no solution exists. What is the maximum gain that can be achieved in this stage?
- 5.44.** Construct the small-signal model of the CE stage shown in Fig. 5.43(a) and calculate the voltage gain. Assume $V_A = \infty$.
- 5.45.** Construct the small-signal model of the CE stage shown in Fig. 5.43(a) and prove that the output impedance is equal to R_C if the Early effect is neglected.
- *5.46.** Determine the voltage gain and I/O impedances of the circuits shown in Fig. 5.138. Assume $V_A = \infty$.
- *5.47.** Compute the voltage gain the I/O impedances of the circuits depicted in Fig. 5.139. Assume $V_A = \infty$.
- *5.48.** Using a small-signal equivalent circuit, compute the output impedance of a degenerated CE stage with $V_A < \infty$. Assume $\beta \gg 1$.
- *5.49.** Compare the output impedances of the circuits illustrated in Fig. 5.140. Assume $\beta \gg 1$.



- *5.50.** Calculate the output impedance of the circuits shown in Fig. 5.141. Assume $\beta \gg 1$.
- *5.51.** Writing $r_\pi = \beta V_T / I_C$, expand Eq. (5.217) and prove that the result remains close to r_π if $I_B R_B \gg V_T$ (which is valid because V_{CC} and V_{BE} typically differ by about 0.5 V or higher).

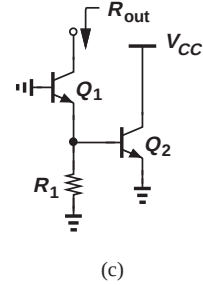
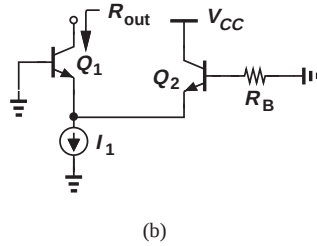
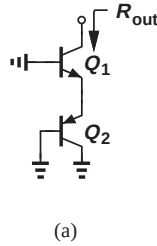


Figure 5.141

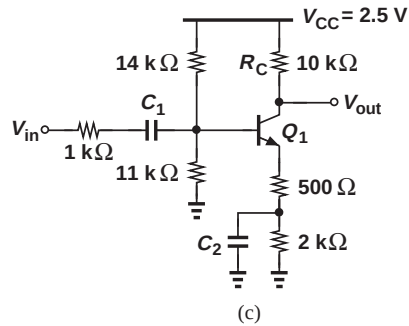
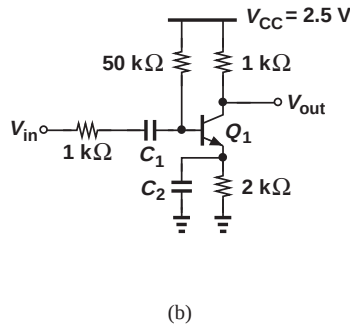
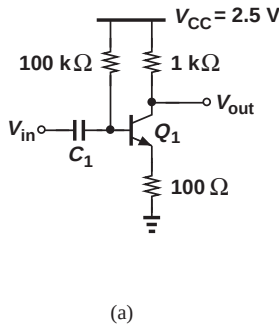


Figure 5.142

Section 5.3.2 Common-Base Topology

- 5.54.** The common-base stage of Fig. 5.143 is biased with a collector current of 2 mA. Assume $V_A = \infty$.
- (a) Calculate the voltage gain and I/O impedances of the circuit.
- (b) How should V_B and R_C be chosen to maximize the voltage gain with a bias current of 2 mA?

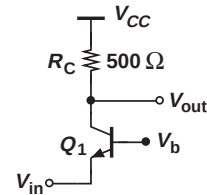


Figure 5.143

- 5.55.** Determine the voltage gain of the circuits shown in Fig. 5.144. Assume $V_A = \infty$.
- *5.56.** Compute the input impedance of the stages depicted in Fig. 5.145. Assume $V_A = \infty$.

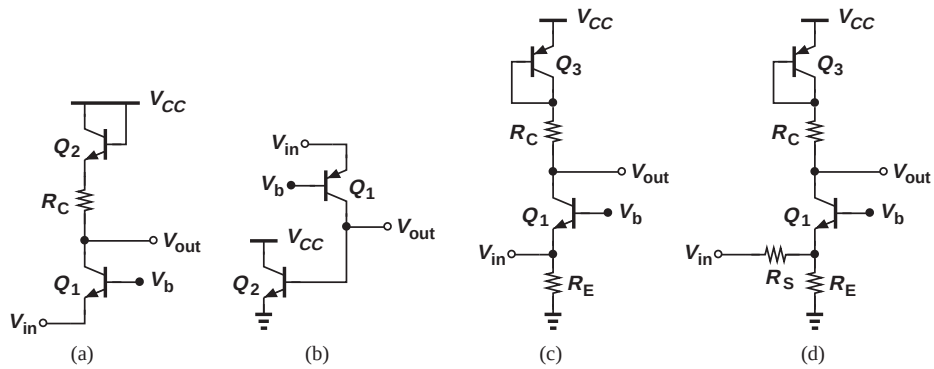


Figure 5.144

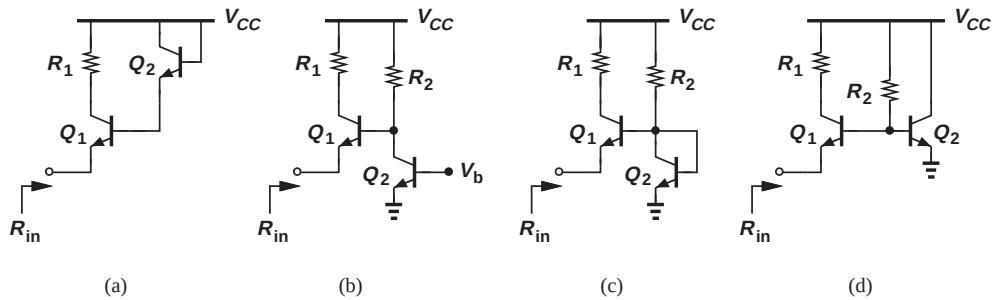


Figure 5.145

5.57. Calculate the voltage gain and I/O impedances of the CB stage shown in Fig. 5.146. Assume $V_A < \infty$.

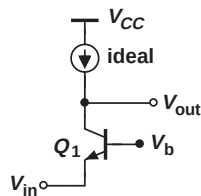


Figure 5.146

(b) Calculate the voltage gain and I/O impedances of the circuit.

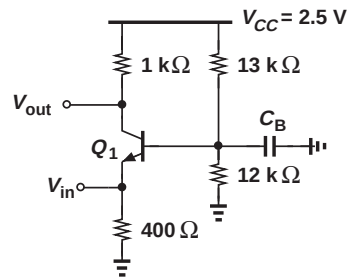


Figure 5.147

5.58. Consider the CB stage depicted in Fig. 5.147, where $\beta = 100$, $I_S = 8 \times 10^{-16}$ A, $V_A = \infty$, and C_B is very large. (a) Determine the operating point of Q_1 .

5.59. Repeat Problem 5.58 for $C_B = 0$.

***5.60.** Calculate the voltage gain and the I/O impedances of the stage depicted in Fig. 5.148 if $V_A = \infty$ and C_B is very large.

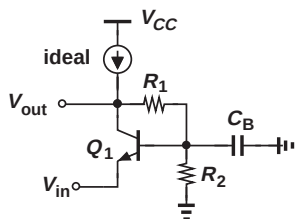


Figure 5.148

- 5.61.** Compute the voltage gain and I/O impedances of the stage shown in Fig. 5.149 if $V_A = \infty$ and C_B is very large.

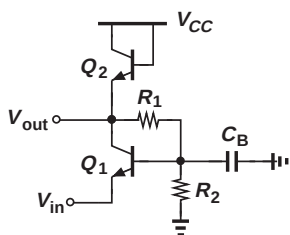


Figure 5.149

- *5.62.** Calculate the voltage gain of the circuit shown in Fig. 5.150 if $V_A < \infty$.

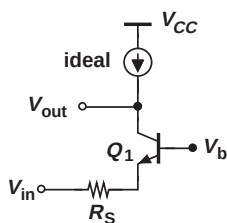


Figure 5.150

- 5.63.** The circuit of Fig. 5.151 provides two outputs. If $I_{S1} = 2I_{S2}$, determine the relationship between v_{out1}/v_{in} and v_{out2}/v_{in} . Assume $V_A = \infty$.

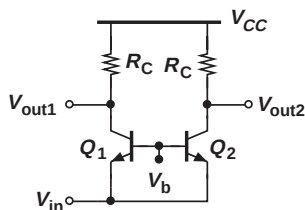


Figure 5.151

- **5.64.** Using a small-signal model, determine the voltage gain of a CB stage with emitter degeneration, a base resistance, and $V_A < \infty$. Assume $\beta \gg 1$.

Section 5.3.3 Emitter Follower

- 5.65.** For $R_E = 100 \Omega$ in Fig. 5.152, determine the bias current of Q_1 such that the gain is equal to 0.8. Assume $V_A = \infty$.

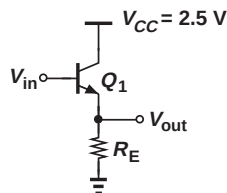


Figure 5.152

- 5.66.** The circuit of Fig. 5.152 must provide an input impedance of greater than $10 \text{ k}\Omega$ with a minimum gain of 0.9. Calculate the required bias current and R_E . Assume $\beta = 100$ and $V_A = \infty$.

- 5.67.** A microphone having an output impedance $R_S = 200 \Omega$ drives an emitter follower as shown in Fig. 5.153. Determine the bias current such that the output impedance does not exceed 5Ω . Assume $\beta = 100$ and $V_A = \infty$.

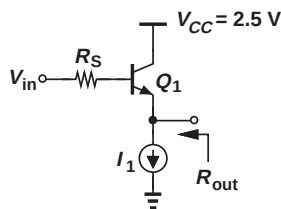


Figure 5.153

- 5.68.** Compute the voltage gain and I/O impedances of the circuits shown in Fig. 5.154. Assume $V_A = \infty$.

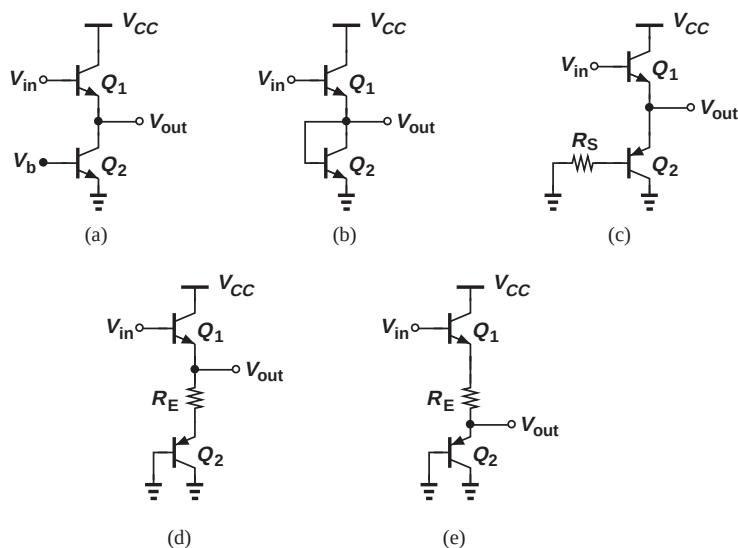


Figure 5.154

***5.69.** Figure 5.155 depicts a “Darlington pair,” where Q_1 plays a role somewhat similar to an emitter follower driving Q_2 . Assume $V_A = \infty$ and the collectors of Q_1 and Q_2 are tied to V_{CC} . Note that $I_{E1} (\approx I_{C1}) = I_{B2} = I_{C2}/\beta$.

- If the emitter of Q_2 is grounded, determine the impedance seen at the base of Q_1 .
- If the base of Q_1 is grounded, calculate the impedance seen at the emitter of Q_2 .
- Compute the current gain of the pair, defined as $(I_{C1} + I_{C2})/I_{B1}$.

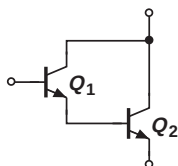


Figure 5.155

5.70. Determine the voltage gain of the follower depicted in Fig. 5.156. Assume $I_S = 7 \times 10^{-16}$ A, $\beta = 100$, and $V_A = 5$ V. (But for bias calculations, assume $V_A = \infty$.) Also, assume the capacitors are very large.

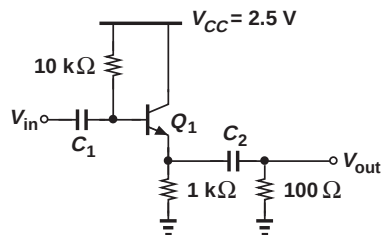


Figure 5.156

***5.71.** In the emitter follower shown in Fig. 5.157, Q_2 serves as a current source for the input device Q_1 .

- Calculate the output impedance of the current source, R_{CS} .
- Replace Q_2 and R_E with the impedance obtained in (a) and compute the voltage gain and I/O impedances of the circuit.

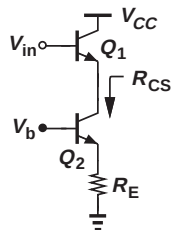


Figure 5.157

5.72. Figure 5.158 illustrates a cascade of an emitter follower and a common-emitter stage. Assume $V_A < \infty$.

- Calculate the input and output impedances of the circuit.
- Determine the voltage gain, $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$.

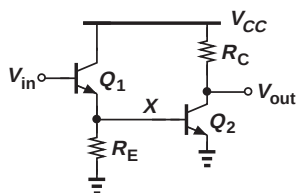


Figure 5.158

***5.73.** Figure 5.159 shows a cascade of an emitter follower and a common-base stage. Assume $V_A = \infty$.

- Calculate the I/O impedances of the circuit.
- Calculate the voltage gain, $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$.

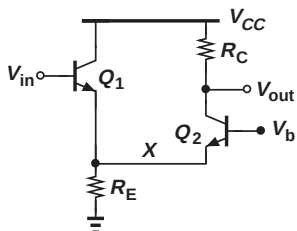


Figure 5.159

Design Problems

In the following problems, unless otherwise stated, assume $\beta = 100$, $I_S = 6 \times 10^{-16} \text{ A}$, and $V_A = \infty$.

5.74. Design the CE stage shown in Fig. 5.160 for a voltage gain of 10, and input impedance of greater than $5 \text{ k}\Omega$, and an output impedance of $1 \text{ k}\Omega$. If the lowest signal frequency of interest is 200 Hz , estimate the minimum allowable value of C_B .

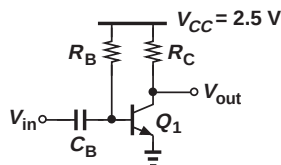


Figure 5.160

5.75. We wish to design the CE stage of Fig. 5.161 for maximum voltage gain but with an output impedance no greater than 500Ω . Allowing the transistor to experience at most 400 mV of base-collector forward bias, design the stage.

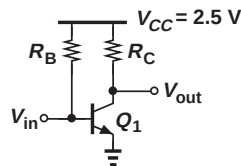


Figure 5.161

5.76. The stage depicted in Fig. 5.161 must achieve maximum input impedance but with a voltage gain of at least 20 and an output impedance of $1 \text{ k}\Omega$. Design the stage.

5.77. The CE stage of Fig. 5.161 must be designed for minimum supply voltage but with a voltage gain of 15 and an output impedance of $2 \text{ k}\Omega$. If the transistor is allowed to sustain a base-collector forward bias of 400 mV , design the stage and calculate the required supply voltage.

5.78. We wish to design the CE stage of Fig. 5.161 for minimum power dissipation. If the voltage gain must be equal to A_0 , determine the trade-off between the power dissipation and the output impedance of the circuit.

5.79. Design the CE stage of Fig. 5.161 for a power budget of 1 mW and a voltage gain of 20.

5.80. Design the degenerated CE stage of Fig. 5.162 for a voltage gain of 5 and an output impedance of 500Ω . Assume R_E sustains a voltage drop of 300 mV and the current flowing through R_1 is approximately 10 times the base current.

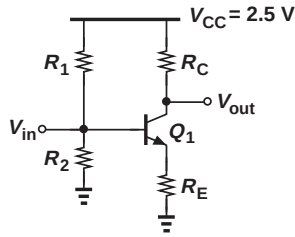


Figure 5.162

- 5.81.** The stage of Fig. 5.162 must be designed for maximum voltage gain but an output impedance of no greater than $1\text{ k}\Omega$. Design the circuit, assuming that R_E sustains 200 mV , the current flowing through R_1 is approximately 10 times the base current, and Q_1 experiences a maximum base-collector forward bias of 400 mV .
- 5.82.** Design the stage of Fig. 5.162 for a power budget of 5 mW , a voltage gain of 5, and a voltage drop of 200 mV across R_E . Assume the current flowing through R_1 is approximately 10 times the base current.
- 5.83.** Design the common-base stage shown in Fig. 5.163 for a voltage gain of 20 and an input impedance of $50\text{ }\Omega$. Assume a voltage drop of $10V_T = 260\text{ mV}$ across R_E so that this resistor does not affect the input impedance significantly. Also, assume the current flowing through R_1 is approximately 10 times the base current, and the lowest frequency of interest is 200 Hz .

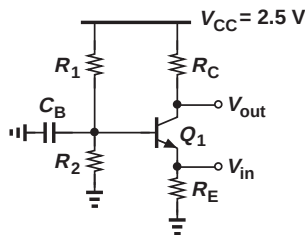


Figure 5.163

- 5.84.** The CB amplifier of Fig. 5.163 must achieve a voltage gain of 8 with an output impedance of $500\text{ }\Omega$. Design the circuit with the same assumptions as those in Problem 5.83.
- 5.85.** We wish to design the CB stage of Fig. 5.163 for an output impedance of $200\text{ }\Omega$ and a voltage gain of 20. What is the minimum

required power dissipation? Make the same assumptions as those in Problem 5.83.

- 5.86.** Design the CB amplifier of Fig. 5.163 for a power budget of 5 mW and a voltage gain of 10. Make the same assumptions as those in Problem 5.83.
- 5.87.** Design the CB stage of Fig. 5.163 for the minimum supply voltage if an input impedance of $50\text{ }\Omega$ and a voltage gain of 20 are required. Make the same assumptions as those in Problem 5.83.
- 5.88.** Design the emitter follower shown in Fig. 5.164 for a voltage gain of 0.85 and an input impedance of greater than $10\text{ k}\Omega$. Assume $R_L = 200\text{ }\Omega$.

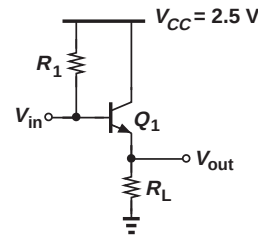


Figure 5.164

- 5.89.** The follower of Fig. 5.164 must consume 5 mW of power while achieving a voltage gain of 0.9. What is the minimum load resistance, R_L , that it can drive?
- 5.90.** The follower shown in Fig. 5.165 must drive a load resistance, $R_L = 50\text{ }\Omega$, with a voltage gain of 0.8. Design the circuit assuming that the lowest frequency of interest is 100 MHz . (Hint: select the voltage drop across R_E to be much greater than V_T so that this resistor does not affect the voltage gain significantly.)

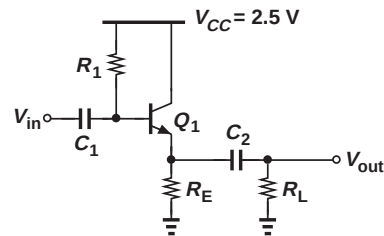


Figure 5.165

SPICE PROBLEMS

In the following problems, assume $I_{S,npn} = 5 \times 10^{-16}$ A, $\beta_{npn} = 100$, $V_{A,npn} = 5$ V, $I_{S,pnp} = 8 \times 10^{-16}$ A, $\beta_{pnp} = 50$, $V_{A,pnp} = 3.5$ V.

5.91. The common-emitter shown in Fig. 5.166 must amplify signals in the range of 1 MHz to 100 MHz.

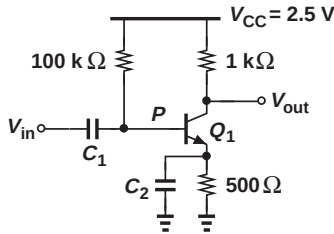


Figure 5.166

- Using the .op command, determine the bias conditions of Q_1 and verify that it operates in the active region.
 - Running an ac analysis, choose the value of C_1 such that $|V_P/V_{in}| \approx 0.99$ at 1 MHz. This ensures that C_1 acts as a short circuit at all frequencies of interest.
 - Plot $|V_{out}/V_{in}|$ as a function of frequency for several values of C_2 , e.g., 1 μ F, 1 nF, and 1 pF. Determine the value of C_2 such that the gain of the circuit at 10 MHz is only 2% below its maximum (i.e., for $C_2 = 1$ μ F).
 - With the proper value of C_2 found in (c), determine the input impedance of the circuit at 10 MHz. (One approach is to insert a resistor in series with V_{in} and adjust its value until V_P/V_{in} or V_{out}/V_{in} drops by a factor of two.)
- 5.92.** Predicting an output impedance of about 1 k Ω for the stage shown in Fig. 5.166, a student constructs the circuit depicted in Fig. 5.167, where V_X represents an ac source with zero dc value. Unfortunately, V_N/V_X is far from 0.5. Explain why.

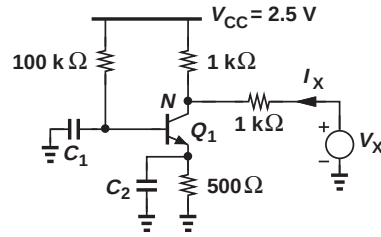


Figure 5.167

5.93. Consider the self-biased stage shown in Fig. 5.168.

- Determine the bias conditions of Q_1 .
- Select the value of C_1 such that it operates as nearly a short circuit (e.g., $|V_P/V_{in}| \approx 0.99$) at 10 MHz.
- Compute the voltage gain of the circuit at 10 MHz.
- Determine the input impedance of the circuit at 10 MHz.
- Suppose the supply voltage is provided by an aging battery. How much can V_{CC} fall while the gain of the circuit degrades by only 5%?

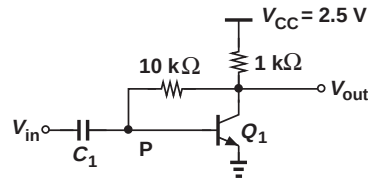


Figure 5.168

5.94. Repeat Problem 5.93 for the stage illustrated in Fig. 5.169. Which one of the two circuits is less sensitive to supply variations?

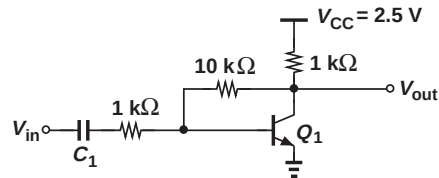


Figure 5.169

5.95. The amplifier shown in Fig. 5.170 employs an emitter follower to drive a $50\text{-}\Omega$ load at a frequency of 100 MHz .

(a) Determine the value of R_{E1} such that Q_2 carries a bias current of 2 mA .

(b) Determine the minimum acceptable value of C_1 , C_2 , and C_3 if each one is to degrade the gain by less than 1% .

(c) What is the signal attenuation of the emitter follower? Does the overall gain increase if R_{G2} is reduced to $100\text{ }\Omega$? Why?

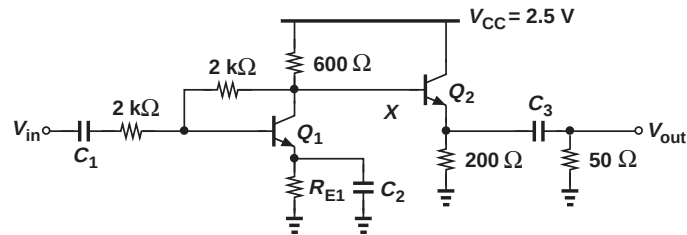


Figure 5.170

Physics of MOS Transistors

PROBLEMS

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, and $V_{TH} = 0.4 \text{ V}$ for NMOS devices and -0.4 V for PMOS devices.

Sec. 6.2 Operation of MOSFET

- *6.1. Two identical MOSFETs are placed in series as shown in Fig. 6.36. If both devices operate as resistors, explain intuitively why

this combination is equivalent to a single transistor, M_{eq} . What are the width and length of M_{eq} ?

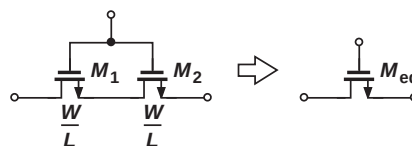


Figure 6.36

- 6.2.** Referring to Fig. 6.11 and assuming that $V_D > 0$,
- Sketch the electron density in the channel as a function of x .
 - Sketch the local resistance of the channel (per unit length) as a function of x .
- 6.3.** Calculate the total charge stored in the channel of an NMOS device if $C_{ox} = 10 \text{ fF}/\mu\text{m}^2$, $W = 5 \mu\text{m}$, $L = 0.1 \mu\text{m}$, and $V_{GS} - V_{TH} = 1 \text{ V}$. Assume $V_{DS} = 0$.
- *6.4.** Consider a MOSFET experiencing pinch-off near the drain. Equation (6.4) indicates that the charge density and carrier velocity must change in opposite directions if the current remains constant. How can this relationship be interpreted at the pinch-off point, where the charge density approaches zero?
- 6.5.** Assuming I_D is constant, solve Eq. (6.7) to obtain an expression for $V(x)$. Plot both $V(x)$ and dV/dx as a function of x for different values of W or V_{TH} .
- *6.6.** The drain current of a MOSFET in the triode region is expressed as

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]. \quad (6.77)$$

Suppose the values of $\mu_n C_{ox}$ and W/L are unknown. Is it possible to determine these quantities by applying different values of $V_{GS} - V_{TH}$ and V_{DS} and measuring I_D ?

- 6.7.** An NMOS device carries 1 mA with $V_{GS} - V_{TH} = 0.6 \text{ V}$ and 1.6 mA with $V_{GS} - V_{TH} = 0.8 \text{ V}$. If the device operates in the triode region, calculate V_{DS} and W/L .
- *6.8.** Compute the transconductance of a MOSFET operating in the triode region. Define $g_m = \partial I_D / \partial V_{GS}$ for a constant V_{DS} . Explain why $g_m = 0$ for $V_{DS} = 0$.
- 6.9.** For a MOS transistor biased in the triode region, we can define an incremental drain-source resistance as

$$r_{DS,tri} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1}. \quad (6.78)$$

Derive an expression for this quantity.

- 6.10.** We wish to use an NMOS transistor as a variable resistor with $R_{on} = 500 \Omega$ at

$V_{GS} = 1 \text{ V}$ and $R_{on} = 400 \Omega$ at $V_{GS} = 1.5 \text{ V}$. Explain why this is not possible.

- 6.11.** An NMOS device operating with a small drain-source voltage serves as a resistor. If the supply voltage is 1.8 V, what is the minimum on-resistance that can be achieved with $W/L = 20$?
- 6.12.** It is possible to define an “intrinsic time constant” for a MOSFET operating as a resistor:

$$\tau = R_{on} C_{GS}, \quad (6.79)$$

where $C_{GS} = W L C_{ox}$. Obtain an expression for τ and explain what the circuit designer must do to minimize the time constant.

- 6.13.** In the circuit of Fig. 6.37, M_1 serves as an electronic switch. If $V_{in} \approx 0$, determine W/L such that the circuit attenuates the signal by only 5%. Assume $V_G = 1.8 \text{ V}$ and $R_L = 100 \Omega$.

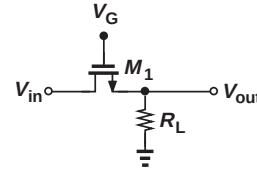


Figure 6.37

- 6.14.** In the circuit of Fig. 6.37, the input is a small sinusoid superimposed on a dc level: $V_{in} = V_0 \cos \omega t + V_1$, where V_0 is on the order of a few millivolts.
- For $V_1 = 0$, obtain W/L in terms of R_L and other parameters so that $V_{out} = 0.95 V_{in}$.
 - Repeat part (a) for $V_1 = 0.5 \text{ V}$. Compare the results.
- 6.15.** For an NMOS device, plot I_D as a function of V_{GS} for different values of V_{DS} .
- 6.16.** In Fig. 6.17, explain why the peaks of the parabolas lie on a parabola themselves.
- 6.17.** For MOS devices with very short channel lengths, the square-law behavior is not valid, and we may instead write:

$$I_D = W C_{ox} (V_{GS} - V_{TH}) v_{sat}, \quad (6.80)$$

where v_{sat} is a relatively constant velocity. Determine the transconductance of such a device.

6.18. Advanced MOS devices do not follow the square-law behavior expressed by Eq. (6.17). A somewhat better approximation is:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^\alpha, \quad (6.81)$$

where α is less than 2. Determine the transconductance of such a device.

***6.19.** Determine the region of operation of M_1 in each of the circuits shown in Fig. 6.38.

***6.20.** Determine the region of operation of M_1 in each of the circuits shown in Fig. 6.39.

6.21. Two current sources realized by identical MOSFETs (Fig. 6.40) match to within 1%, i.e., $0.99I_{D2} < I_{D1} < 1.01I_{D2}$. If $V_{DS1} = 0.5$ V and $V_{DS2} = 1$ V, what is the maximum tolerable value of λ ?

6.22. Assume $\lambda = 0$, compute W/L of M_1 in Fig. 6.41 such that the device operates at the edge of saturation.

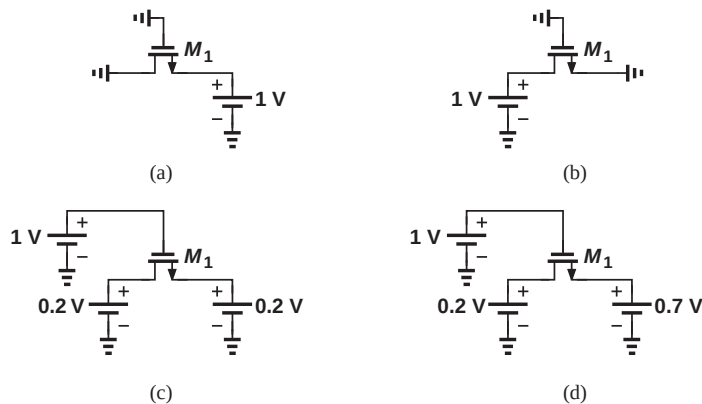


Figure 6.38

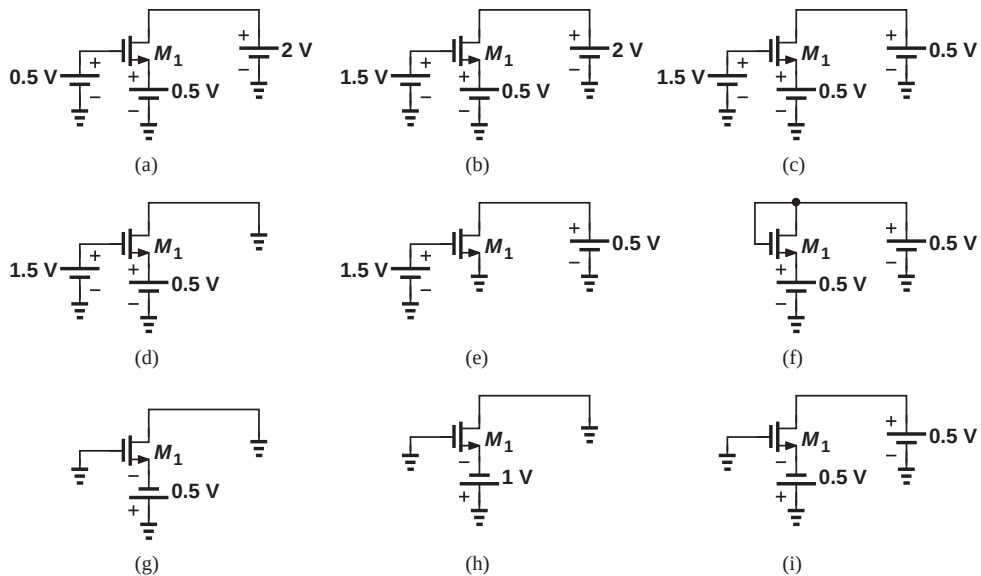


Figure 6.39

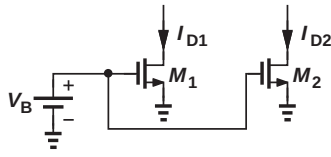


Figure 6.40

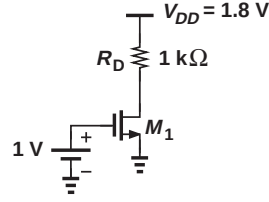


Figure 6.41

- 6.23.** Using the value of W/L found in Problem 6.22, explain what happens if the gate oxide thickness is doubled due to a manufacturing error.
- 6.24.** In the Fig. 6.42, what is the minimum allowable value of V_{DD} if M_1 must not enter the triode region? Assume $\lambda = 0$.

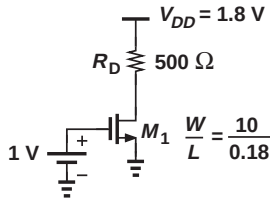


Figure 6.42

- 6.25.** Calculate the bias current of M_1 in Fig. 6.43 if $\lambda = 0$.

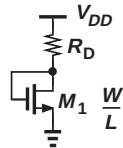


Figure 6.43

- 6.26.** Compute the value of W/L for M_1 in Fig. 6.44 for a bias current of I_1 . Assume $\lambda = 0$.

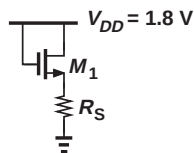


Figure 6.44

- *6.27.** In Fig. 6.45, derive a relationship among the circuit parameters that guarantees M_1 operates at the edge of saturation. Assume $\lambda = 0$.

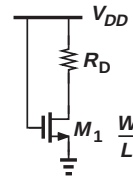


Figure 6.45

- **6.28.** Sketch I_X as a function of V_X for the circuits shown in Fig. 6.46. Assume V_X goes from 0 to $V_{DD} = 1.8$ V. Also, $\lambda = 0$. Determine at what value of V_X the device changes its region of operation.

- 6.29.** Assuming $W/L = 10/0.18$ $\lambda = 0.1$ V⁻¹, and $V_{DD} = 1.8$ V, calculate the drain current of M_1 in Fig. 6.47.

- 6.30.** In the circuit of Fig. 6.48, $W/L = 20/0.18$ and $\lambda = 0.1$ V⁻¹. What value of V_B places the transistor at the edge of saturation?

- 6.31.** An NMOS device operating in saturation with $\lambda = 0$ must provide a transconductance of $1/(50 \Omega)$.

- Determine W/L if $I_D = 0.5$ mA.
- Determine W/L if $V_{GS} - V_{TH} = 0.5$ V.
- Determine I_D if $V_{GS} - V_{TH} = 0.5$ V.

- **6.32.** Determine how the transconductance of a MOSFET (operating in saturation) changes if

- W/L is doubled but I_D remains constant.
- $V_{GS} - V_{TH}$ is doubled but I_D remains constant.
- I_D is doubled but W/L remains constant.
- I_D is doubled but $V_{GS} - V_{TH}$ remains constant.

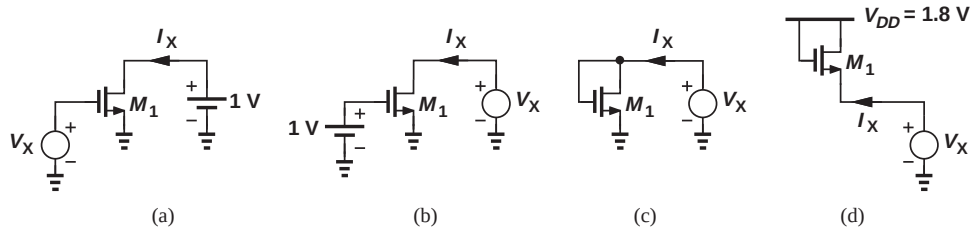


Figure 6.46

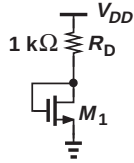


Figure 6.47

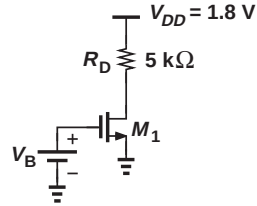
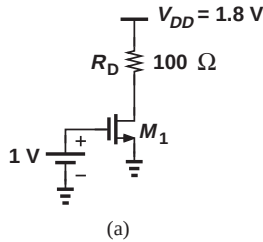
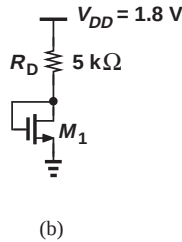


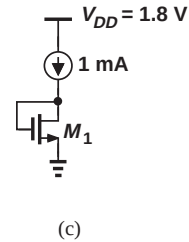
Figure 6.48



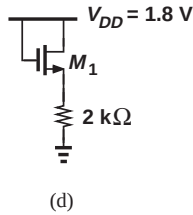
(a)



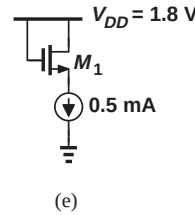
(b)



(c)



(d)



(e)

Figure 6.49

- 6.33.** The “intrinsic gain” of a MOSFET operating in saturation is defined as $g_m r_O$. Derive an expression for $g_m r_O$ and plot the result as a function of I_D . Assume V_{DS} is constant.
- 6.34.** If $\lambda = 0.1 \text{ V}^{-1}$ and $W/L = 20/0.18$, construct the small-signal model of each of the circuits shown in Fig. 6.49.
- *6.35.** Assuming a constant V_{DS} , plot the intrinsic gain, $g_m r_O$, of a MOSFET
- as a function of $V_{GS} - V_{TH}$ if I_D is constant.
 - as a function of I_D if $V_{GS} - V_{TH}$ is constant.
- 6.36.** An NMOS device with $\lambda = 0.1 \text{ V}^{-1}$ must provide a $g_m r_O$ of 20 with $V_{DS} = 1.5 \text{ V}$. Determine the required value of W/L if $I_D = 0.5 \text{ mA}$.
- 6.37.** Repeat Problem 6.36 for $\lambda = 0.2 \text{ V}^{-1}$.
- 6.38.** Construct the small-signal model of the circuits depicted in Fig. 6.50. Assume all transistors operate in saturation and $\lambda \neq 0$.

Sec. 6.4 PMOS Transistor

- *6.39.** Determine the region of operation of M_1 in each circuit shown in Fig. 6.51.
- *6.40.** Determine the region of operation of M_1 in each circuit shown in Fig. 6.52.

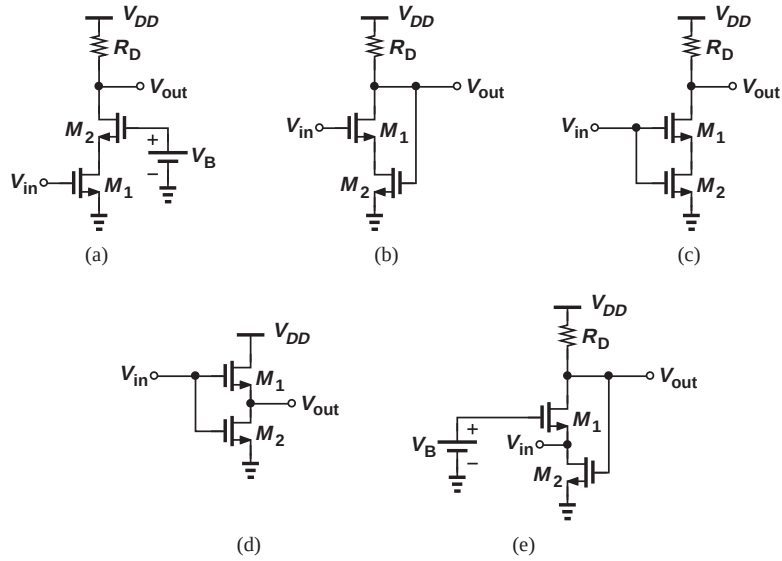


Figure 6.50

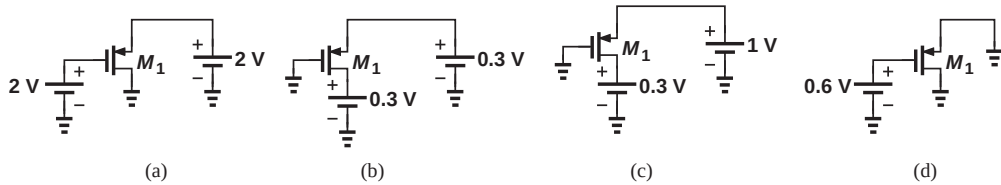


Figure 6.51

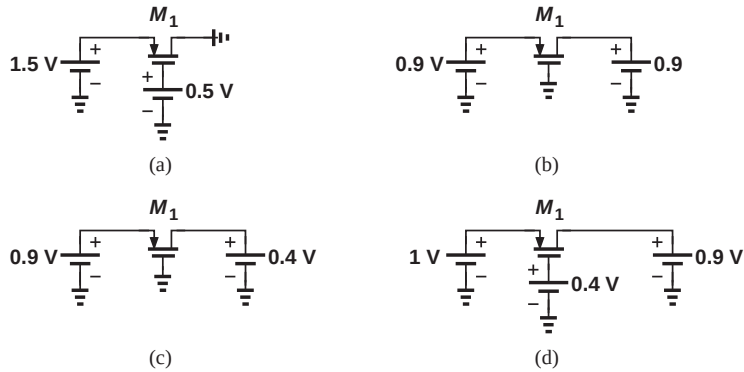


Figure 6.52

- 6.41.** If $\lambda = 0$, what value of W/L places M_1 at the edge of saturation in Fig. 6.53?
- 6.42.** With the value of W/L obtained in Problem 6.41, what happens if V_B changes to $+0.8$ V?
- 6.43.** If $W/L = 10/0.18$ and $\lambda = 0$, determine the operating point of M_1 in each circuit depicted in Fig. 6.54.
- 6.44.** Sketch I_X as a function of V_X for the circuits shown in Fig. 6.55. Assume V_X goes from 0 to $V_{DD} = 1.8$ V. Also, $\lambda = 0$. Determine at what value of V_X the device changes its region of operation.
- 6.45.** Construct the small-signal model of each circuit shown in Fig. 6.56 if all of the transistors operate in saturation and $\lambda \neq 0$.

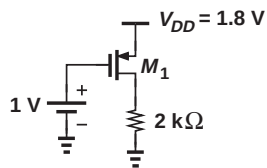
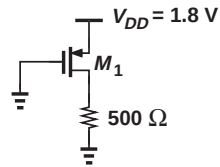
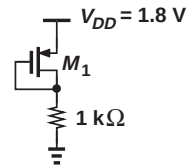


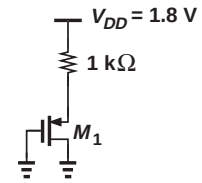
Figure 6.53



(a)

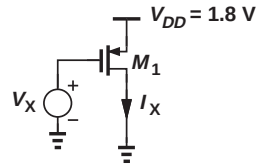


(b)

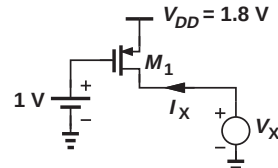


(c)

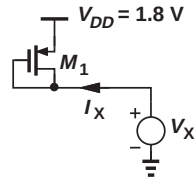
Figure 6.54



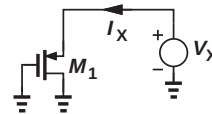
(a)



(b)

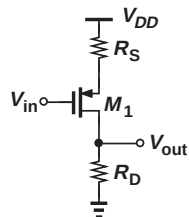


(c)

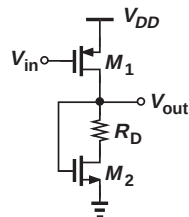


(d)

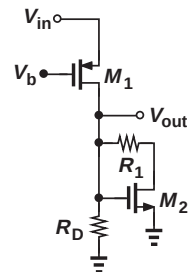
Figure 6.55



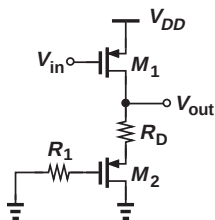
(a)



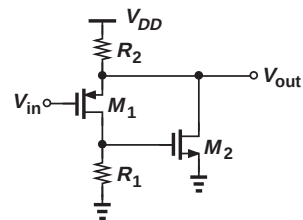
(b)



(c)



(d)



(e)

Figure 6.56

- **6.46.** Consider the circuit depicted in Fig. 6.57, where M_1 and M_2 operate in saturation and exhibit channel-length modulation coefficients λ_n and λ_p , respectively.
- Construct the small-signal equivalent circuit and explain why M_1 and M_2 appear in “parallel.”
 - Determine the small-signal voltage gain of the circuit.

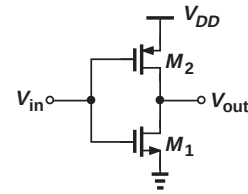


Figure 6.57

SPICE PROBLEMS

In the following problems, use the MOS models and source/drain dimensions given in Appendix A. Assume the substrates of NMOS and PMOS devices are tied to ground and V_{DD} , respectively.

- 6.47.** For the circuit shown in Fig. 6.58, plot V_X as a function of I_X for $0 < I_X < 3$ mA. Explain the sharp change in V_X as I_X exceeds a certain value.

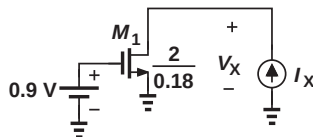


Figure 6.58

- 6.48.** Plot the input/output characteristic of the stage shown in Fig. 6.59 for $0 < V_{in} < 1.8$ V. At what value of V_{in} does the slope (gain) reach a maximum?

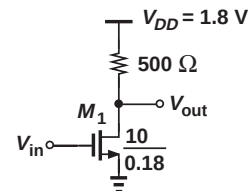


Figure 6.59

- 6.49.** For the arrangements shown in Fig. 6.60, plot I_D as a function of V_X as V_X varies from 0 to 1.8 V. Can we say these two arrangements are equivalent?

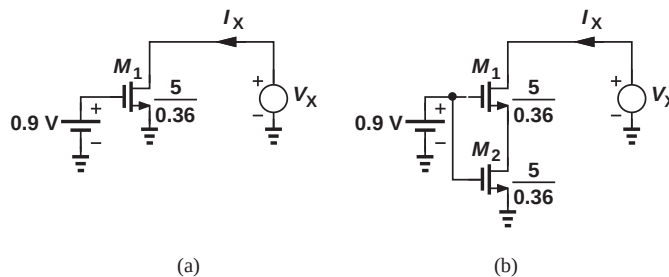


Figure 6.60

6.50. Plot I_X as a function of V_X for the arrangement depicted in Fig. 6.61 as V_X varies from 0 to 1.8 V. Can you explain the behavior of the circuit?

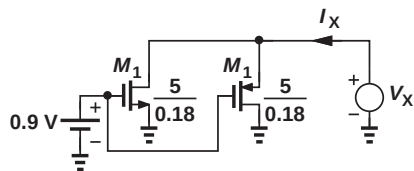


Figure 6.61

6.51. Repeat Problem 6.50 for the circuit illustrated in Fig. 6.62.

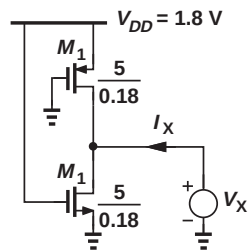
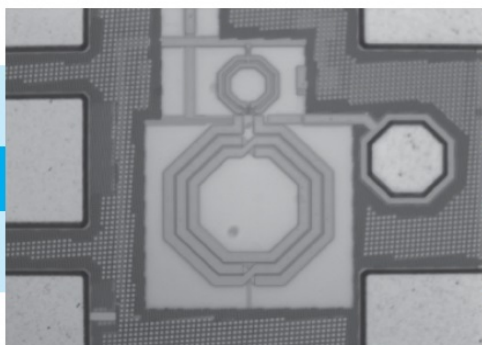


Figure 6.62



7

CMOS Amplifiers

PROBLEMS

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, $\lambda = 0$, and $V_{TH} = 0.4 \text{ V}$ for NMOS devices and -0.4 V for PMOS devices.

Sec. 7.1.2 Biasing

- 7.1.** In the circuit of Fig. 7.39, determine the maximum allowable value of W/L if M_1 must remain in saturation. Assume $\lambda = 0$.

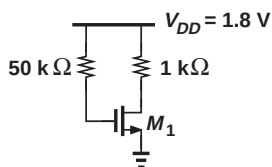


Figure 7.39

- 7.2.** We wish to design the circuit of Fig. 7.40 for a drain current of 1 mA. If $W/L = 20/0.18$, compute R_1 and R_2 such that the input impedance is at least 20 kΩ.

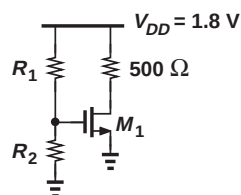


Figure 7.40

- 7.3.** Consider the circuit shown in Fig. 7.41. Calculate the maximum transconductance that M_1 can provide (without going into the triode region.)

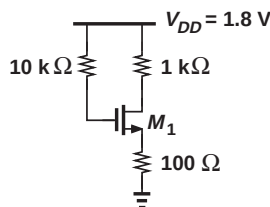


Figure 7.41

7.4. The circuit of Fig. 7.42 must be designed for a voltage drop of 200 mV across R_S .

- Calculate the minimum allowable value of W/L if M_1 must remain in saturation.
- What are the required values of R_1 and R_2 if the input impedance must be at least 30 k Ω ?

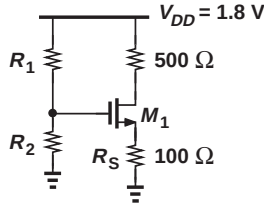


Figure 7.42

7.5. Consider the circuit depicted in Fig. 7.43, where $W/L = 20/0.18$. Assuming the current flowing through R_2 is one-tenth of I_{D1} , calculate the values of R_1 and R_2 so that $I_{D1} = 0.5$ mA.

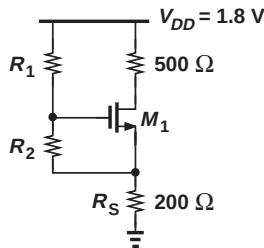


Figure 7.43

7.6. The self-biased stage of Fig. 7.44 must be designed for a drain current of 1 mA. If M_1 is to provide a transconductance of $1/(100 \Omega)$, calculate the required value of R_D .

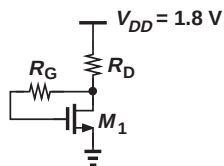


Figure 7.44

7.7. We wish to design the stage in Fig. 7.45 for a drain current of 0.5 mA. If $W/L = 50/0.18$, calculate the values of R_1 and R_2 such that these resistors carry a current equal to one-tenth of I_{D1} .

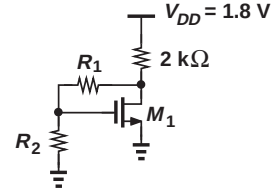


Figure 7.45

***7.8.** Due to a manufacturing error, a parasitic resistor, R_P has appeared in the circuit of Fig. 7.46. We know that circuit samples free from this error exhibit $V_{GS} = V_{DS} + 100$ mV whereas defective samples exhibit $V_{GS} = V_{DS} + 50$ mV. Determine the values of W/L and R_P .

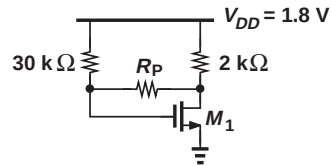


Figure 7.46

***7.9.** Due to a manufacturing error, a parasitic resistor, R_P has appeared in the circuit of Fig. 7.47. We know that circuit samples free from this error exhibit $V_{GS} = V_{DS}$ whereas defective samples exhibit $V_{GS} = V_{DS} + V_{TH}$. Determine the values of W/L and R_P if the drain current is 1 mA without R_P .

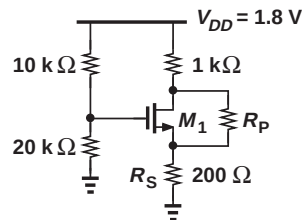


Figure 7.47

Sec. 7.1.3 Realization of Current Sources

7.10. In the circuit of Fig. 7.48, M_1 and M_2 have lengths equal to $0.25\ \mu\text{m}$ and $\lambda = 0.1\ \text{V}^{-1}$. Determine W_1 and W_2 such that $I_X = 2I_Y = 1\ \text{mA}$. Assume $V_{DS1} = V_{DS2} = V_B = 0.8\ \text{V}$. What is the output resistance of each current source?

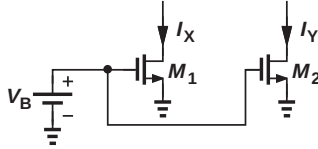


Figure 7.48

7.11. An NMOS current source must be designed for an output resistance of $20\ \text{k}\Omega$ and an output current of $0.5\ \text{mA}$. What is the maximum tolerable value of λ ?

7.12. The two current sources in Fig. 7.49 must be designed for $I_X = I_Y = 0.5\ \text{mA}$. If $V_{B1} = 1\ \text{V}$, $V_{B2} = 1.2\ \text{V}$, $\lambda = 0.1\ \text{V}^{-1}$, and $L_1 = L_2 = 0.25\ \mu\text{m}$, calculate W_1 and W_2 . Compare the output resistances of the two current sources.

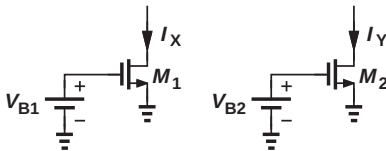


Figure 7.49

7.13. Consider the circuit shown in Fig. 7.50, where $(W/L)_1 = 10/0.18$ and $(W/L)_2 = 30/0.18$. If $\lambda = 0.1\ \text{V}^{-1}$, calculate V_B such that $V_X = 0.9\ \text{V}$.

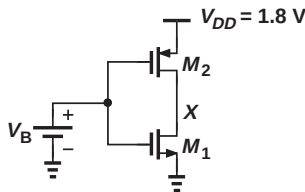


Figure 7.50

7.14. In the circuit of Fig. 7.51, M_1 and M_2 serve as current sources. Calculate I_X and I_Y if $V_B = 1\ \text{V}$ and $W/L = 20/0.25$. How are the output resistances of M_1 and M_2 related?

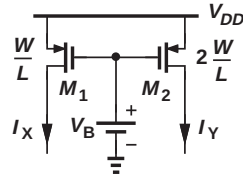


Figure 7.51

***7.15.** A student mistakenly uses the circuit of Fig. 7.52 as a current source. If $W/L = 10/0.25$, $\lambda = 0.1\ \text{V}^{-1}$, $V_{B1} = 0.2\ \text{V}$, and V_X has a dc level of $1.2\ \text{V}$, calculate the impedance seen at the source of M_1 .

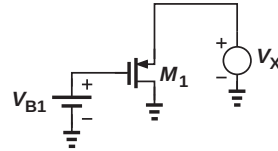


Figure 7.52

***7.16.** In the circuit of Fig. 7.53, $(W/L)_1 = 5/0.18$, $(W/L)_2 = 10/0.18$, $\lambda_1 = 0.1\ \text{V}^{-1}$, and $\lambda_2 = 0.15\ \text{V}^{-1}$.

- Determine V_B such that $I_{D1} = |I_{D2}| = 0.5\ \text{mA}$ for $V_X = 0.9\ \text{V}$.
- Now sketch I_X as a function of V_X as V_X goes from 0 to V_{DD} .

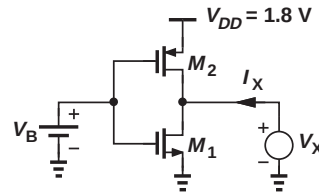


Figure 7.53

Sec. 7.2 Common-Source Stage

7.17. In the common-source stage of Fig. 7.54, $W/L = 30/0.18$ and $\lambda = 0$.

- What gate voltage yields a drain current of $0.5\ \text{mA}$? (Verify that M_1 operates in saturation.)

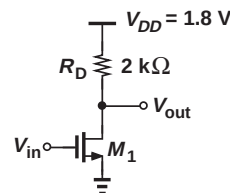


Figure 7.54

- (b) With such a drain bias current, calculate the voltage gain of the stage.

7.18. The circuit of Fig. 7.54 is designed with $W/L = 20/0.18$, $\lambda = 0$, and $I_D = 0.25$ mA.

- (a) Compute the required gate bias voltage.
 (b) With such a gate voltage, how much can W/L be increased while M_1 remains in saturation? What is the maximum voltage gain that can be achieved as W/L increases?

7.19. We wish to design the stage of Fig. 7.55 for a voltage gain of 5 with $W/L \leq 20/0.18$. Determine the required value of R_D if the power dissipation must not exceed 1 mW.

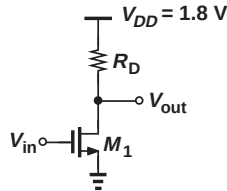


Figure 7.55

7.20. The CS stage of Fig. 7.56 must provide a voltage gain of 10 with a bias current of 0.5 mA. Assume $\lambda_1 = 0.1$ V⁻¹, and $\lambda_2 = 0.15$ V⁻¹.

- (a) Compute the required value of $(W/L)_1$.
 (b) If $(W/L)_2 = 20/0.18$, calculate the required value of V_B .

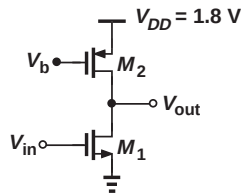


Figure 7.56

7.21. In the stage of Fig. 7.56, M_2 has a long length so that $\lambda_2 \ll \lambda_1$. Calculate the voltage gain if $\lambda_1 = 0.1$ V⁻¹, $(W/L)_1 = 20/0.18$, and $I_D = 1$ mA.

****7.22.** The circuit of Fig. 7.56 is designed for a bias current of I_1 with certain dimensions for M_1 and M_2 . If the width and the length of both transistors are doubled, how does the voltage gain change? Consider two cases:

- (a) the bias current remains constant, or (b) the bias current is doubled.

7.23. The CS stage depicted in Fig. 7.57 must achieve a voltage gain of 15 at a bias current of 0.5 mA. If $\lambda_1 = 0.15$ V⁻¹ and $\lambda_2 = 0.05$ V⁻¹, determine the required value of $(W/L)_2$.

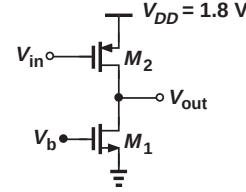


Figure 7.57

7.24. Explain which one of the topologies shown in Fig. 7.58 is preferred.

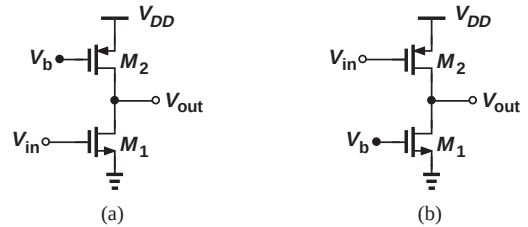


Figure 7.58

7.25. We wish to design the circuit shown in Fig. 7.59 for a voltage gain of 3. If $(W/L)_1 = 20/0.18$, determine $(W/L)_2$. Assume $\lambda = 0$.

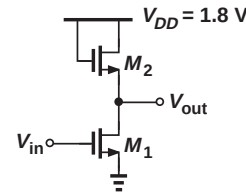


Figure 7.59

7.26. In the circuit of Fig. 7.59, $(W/L)_1 = 10/0.18$ and $I_{D1} = 0.5$ mA.

- (a) If $\lambda = 0$, determine $(W/L)_2$ such that M_1 operates at the edge of saturation.
 (b) Now calculate the voltage gain.
 (c) Explain why this choice of $(W/L)_2$ yields the maximum gain.

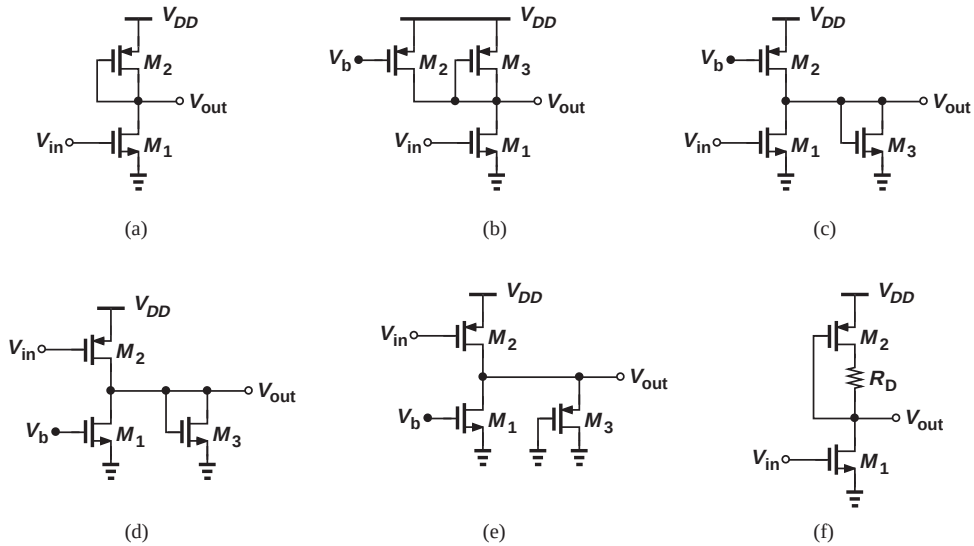


Figure 7.60

7.27. The CS stage of Fig. 7.59 must achieve a voltage gain of 5.

- If $(W/L)_2 = 2/0.18$, compute the required value of $(W/L)_1$.
- What is the maximum allowable bias current if M_1 must operate in saturation?

***7.28.** If $\lambda \neq 0$, determine the voltage gain of the stages shown in Fig. 7.60.

***7.29.** In the circuit of Fig. 7.61, determine the gate voltage such that M_1 operates at the edge of saturation. Assume $\lambda = 0$.

***7.30.** The degenerated CS stage of Fig. 7.61 must provide a voltage gain of 4 with a bias current of 1 mA. Assume a drop of 200 mV across R_S and $\lambda = 0$.

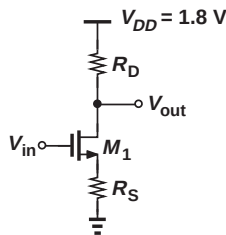


Figure 7.61

- If $R_D = 1 \text{ k}\Omega$, determine the required value of W/L . Does the transistor operate in saturation for this choice of W/L ?
- If $W/L = 50/0.18$, determine the required value of R_D . Does the transistor operate in saturation for this choice of R_D ?

***7.31.** Calculate the voltage gain of the circuits depicted in Fig. 7.62. Assume $\lambda = 0$.

***7.32.** Consider a degenerated CS stage with $\lambda > 0$. Assuming $g_m r_O \gg 1$, calculate the voltage gain of the circuit.

***7.33.** Determine the output impedance of each circuit shown in Fig. 7.63. Assume $\lambda \neq 0$.

7.34. The CS stage of Fig. 7.64 carries a bias current of 1 mA. If $R_D = 1 \text{ k}\Omega$ and $\lambda = 0.1 \text{ V}^{-1}$, compute the required value of W/L for a gate voltage of 1 V. What is the voltage gain of the circuit?

7.35. Repeat Problem 7.34 with $\lambda = 0$ and compare the results.

7.36. An adventurous student decides to try a new circuit topology wherein the input is applied to the drain and the output is sensed at the source (Fig. 7.65). Assume $\lambda \neq 0$, determine the voltage gain of the circuit and discuss the result.

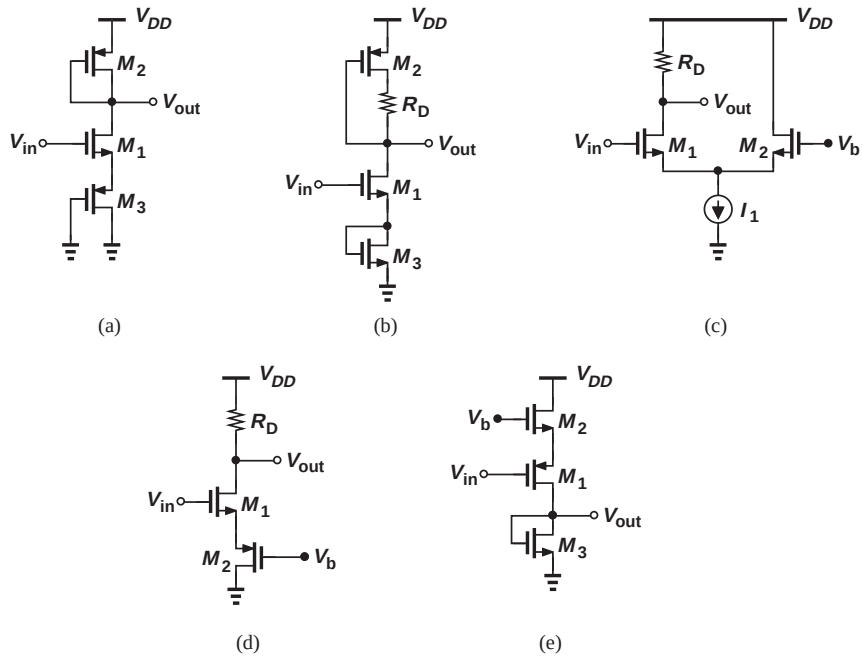


Figure 7.62

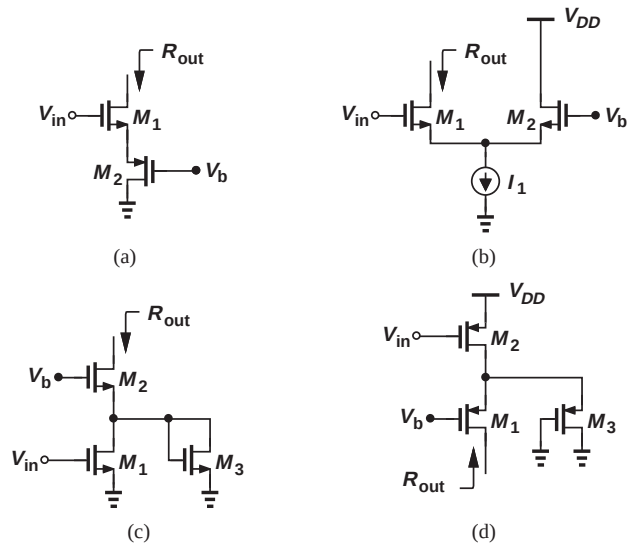


Figure 7.63

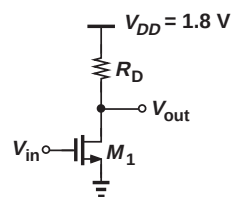


Figure 7.64

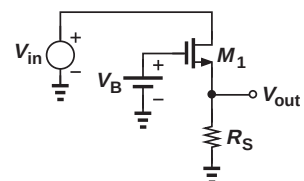


Figure 7.65

7.37. In the common-source stage depicted in Fig. 7.66, the drain current of M_1 is defined by the ideal current source I_1 and remains independent of R_1 and R_2 (why?). Suppose $I_1 = 1$ mA, $R_D = 500$ Ω , $\lambda = 0$, and C_1 is very large.

- Compute the value of W/L to obtain a voltage gain of 5.
- Choose the values of R_1 and R_2 to place the transistor 200 mV away from the triode region while $R_1 + R_2$ draws no more than 0.1 mA from the supply.
- With the values found in (b), what happens if W/L is twice that found in (a)? Consider both the bias conditions (e.g., whether M_1 comes closer to the triode region) and the voltage gain.

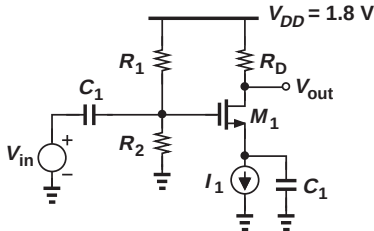


Figure 7.66

7.38. Consider the CS stage shown in Fig. 7.67, where I_1 defines the bias current of M_1 and C_1 is very large.

- If $\lambda = 0$ and $I_1 = 1$ mA, what is the maximum allowable value of R_D for M_1 to remain in saturation?
- With the value found in (a), determine W/L to obtain a voltage gain of 5.

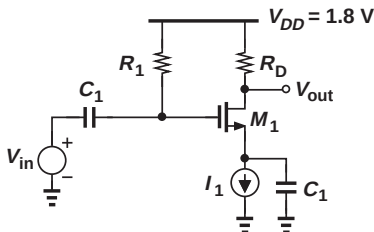


Figure 7.67

Sec. 7.3 Common-Gate Stage

7.39. The common-gate stage shown in Fig. 7.68 must provide a voltage gain of 4 and an input impedance of 50 Ω . If $I_D = 0.5$ mA, and $\lambda = 0$, determine the values of R_D and W/L .

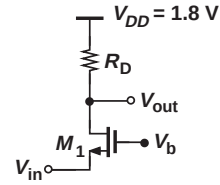


Figure 7.68

7.40. Suppose in Fig. 7.68, $I_D = 0.5$ mA, $\lambda = 0$, and $V_b = 1$ V. Determine the values of W/L and R_D for an input impedance of 50 Ω and maximum voltage gain (while M_1 remains in saturation).

7.41. The CG stage depicted in Fig. 7.69 must provide an input impedance of 50 Ω and an output impedance of 500 Ω . Assume $\lambda = 0$.

- What is the maximum allowable value of I_D ?
- With the value obtained in (a), calculate the required value of W/L .
- Compute the voltage gain.

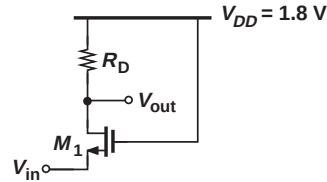


Figure 7.69

***7.42.** A CG stage with a source resistance of R_S employs a MOSFET with $\lambda > 0$. Assuming $g_m r_o \gg 1$, calculate the voltage gain of the circuit.

7.43. The CG amplifier shown in Fig. 7.70 is biased by means of $I_1 = 1$ mA. Assume $\lambda = 0$ and C_1 is very large.

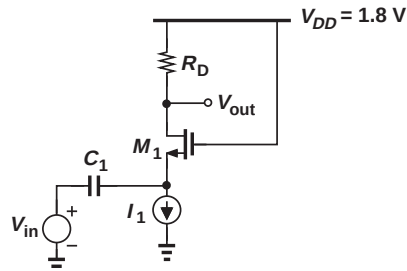


Figure 7.70

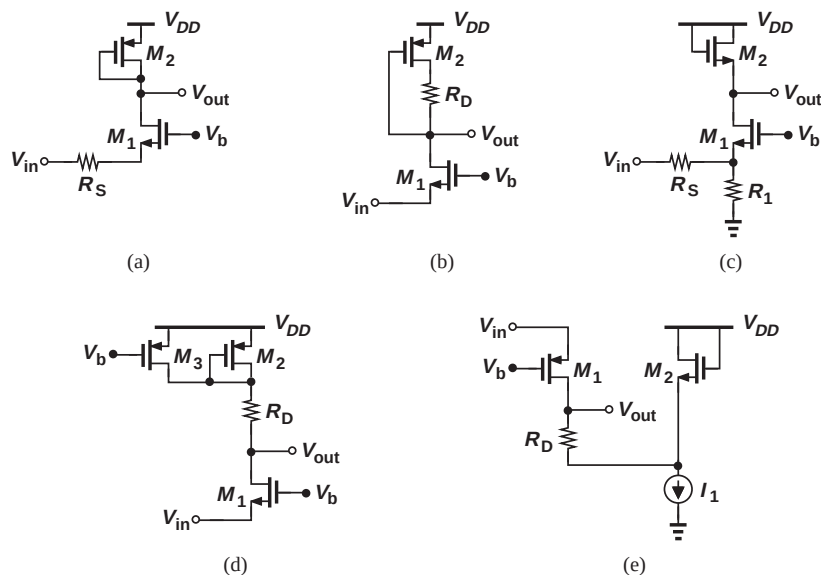


Figure 7.71

- (a) What value of R_D places the transistor M_1 100 mV away from the triode region?
 (b) What is the required W/L if the circuit must provide a voltage gain of 5 with the value of R_D obtained in (a)?

***7.44.** Determine the voltage gain of each stage depicted in Fig. 7.71. Assume $\lambda = 0$.

7.45. Consider the circuit of Fig. 7.72, where a common-source stage (M_1 and R_{D1}) is followed by a common-gate stage (M_2 and R_{D2}).

- (a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$ and assuming $\lambda = 0$, compute the overall voltage gain.
 (b) Simplify the result obtained in (a) if $R_{D1} \rightarrow \infty$. Explain why this result is to be expected.

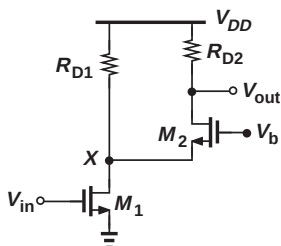


Figure 7.72

7.46. Repeat Problem 7.45 for the circuit shown in Fig. 7.73.

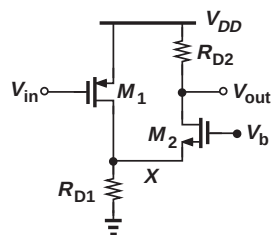


Figure 7.73

7.47. Assuming $\lambda = 0$, calculate the voltage gain of the circuit shown in Fig. 7.74. Explain why this stage is *not* a common-gate amplifier.

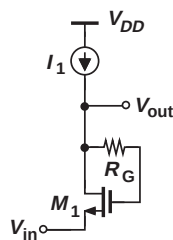


Figure 7.74

- 7.48.** Calculate the voltage gain of the stage depicted in Fig. 7.75. Assume $\lambda = 0$ and the capacitors are very large.

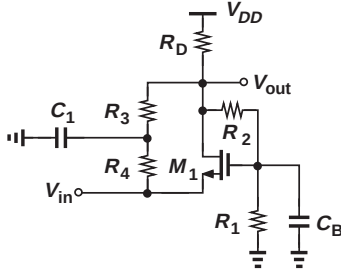


Figure 7.75

Sec. 7.4 Source Follower

- 7.49.** The source follower shown in Fig. 7.76 is biased through R_G . Calculate the voltage gain if $W/L = 20/0.18$ and $\lambda = 0.1 \text{ V}^{-1}$.

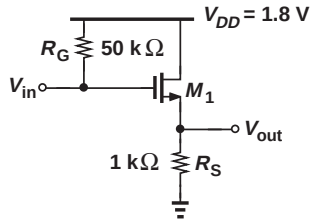


Figure 7.76

- 7.50.** We wish to design the source follower shown in Fig. 7.77 for a voltage gain of 0.8. If $W/L = 30/0.18$ and $\lambda = 0$, determine the required gate bias voltage.

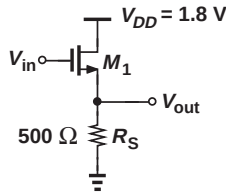


Figure 7.77

- 7.51.** The source follower of Fig. 7.77 is to be designed with a maximum bias gate voltage of 1.8 V. Compute the required value of W/L for a voltage gain of 0.8 if $\lambda = 0$.
- 7.52.** The source follower depicted in Fig. 7.78 employs a current source. Determine the values of I_1 and W/L if the circuit must provide an output impedance less than 100Ω with $V_{GS} = 0.9 \text{ V}$. Assume $\lambda = 0$.

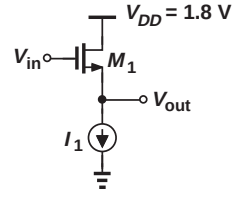


Figure 7.78

- 7.53.** The circuit of Fig. 7.78 must exhibit an output impedance of less than 50Ω with a power budget of 2 mW. Determine the required value of W/L . Assume $\lambda = 0$.
- 7.54.** We wish to design the source follower of Fig. 7.79 for a voltage gain of 0.8 with a power budget of 3 mW. Compute the required value of W/L . Assume C_1 is very large and $\lambda = 0$.

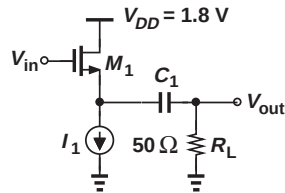


Figure 7.79

- *7.55.** Determine the voltage gain of the stages shown in Fig. 7.80. Assume $\lambda \neq 0$.
- *7.56.** Consider the circuit shown in Fig. 7.81, where a source follower (M_1 and I_1) precedes a common-gate stage (M_2 and R_D).
- (a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$, compute the overall voltage gain.
- (b) Simplify the result obtained in (a) if $g_{m1} = g_{m2}$.

Design Problems

In the following problems, unless otherwise stated, assume $\lambda = 0$.

- 7.57.** Design the CS stage shown in Fig. 7.82 for a voltage gain of 5 and an output impedance of $1 \text{ k}\Omega$. Bias the transistor so that it operates 100 mV away from the triode region. Assume the capacitors are very large and $R_D = 10 \text{ k}\Omega$.

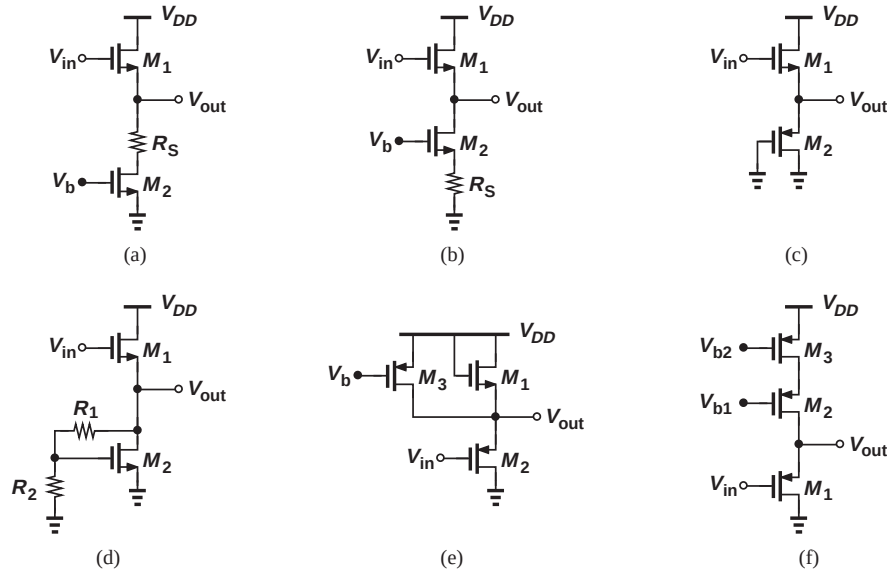


Figure 7.80

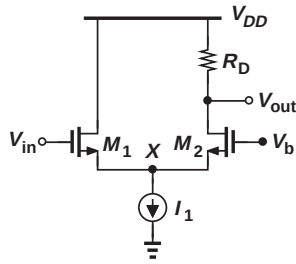


Figure 7.81

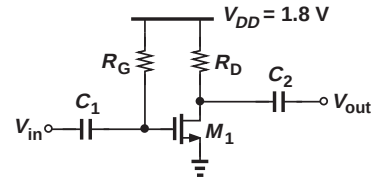


Figure 7.82

- 7.58.** The CS amplifier of Fig. 7.82 must be designed for a voltage gain of 5 with a power budget of 2 mW. If $R_D I_D = 1 \text{ V}$, determine the required value of W/L . Make the same assumptions as those in Problem 7.57.
- 7.59.** We wish to design the CS stage of Fig. 7.82 for maximum voltage gain but with $W/L \leq 50/0.18$ and a maximum output impedance of 500Ω . Determine the required current. Make the same assumptions as those in Problem 7.57.
- 7.60.** The degenerated stage depicted in Fig. 7.83 must provide a voltage gain of 4 with a power budget of 2 mW while the voltage drop across R_S is equal to 200 mV. If the overdrive voltage of the transistor must not exceed 300 mV and $R_1 + R_2$

must consume less than 5% of the allocated power, design the circuit. Make the same assumptions as those in Problem 7.57.

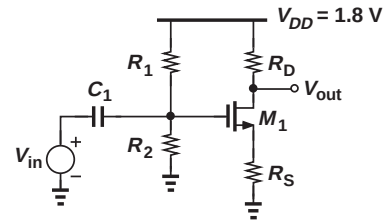


Figure 7.83

- 7.61.** Design the circuit of Fig. 7.83 for a voltage gain of 5 and a power budget of 6 mW. Assume the voltage drop across R_S is equal to the overdrive voltage of the transistor and $R_D = 200 \Omega$.

- 7.62.** The circuit shown in Fig. 7.84 must provide a voltage gain of 6, with C_S serving as a low impedance at the frequencies of interest. Assuming a power budget of 2 mW and an input impedance of 20 k Ω , design the circuit such that M_1 operates 200 mV away from the triode region. Select the values of C_1 and C_S so that their impedance is negligible at 1 MHz.

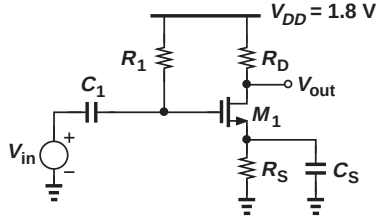


Figure 7.84

- 7.63.** In the circuit of Fig. 7.85, M_2 serves as a current source. Design the stage for a voltage gain of 20 and a power budget of 2 mW. Assume $\lambda = 0.1 \text{ V}^{-1}$ for both transistors and the maximum allowable level at the output is 1.5 V (i.e., M_2 must remain in saturation if $V_{out} \leq 1.5 \text{ V}$).

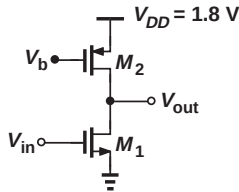


Figure 7.85

- 7.64.** Consider the circuit shown in Fig. 7.86, where C_B is very large and $\lambda_n = 0.5\lambda_p = 0.1 \text{ V}^{-1}$.

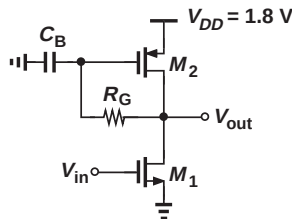


Figure 7.86

- (a) Calculate the voltage gain.
 (b) Design the circuit for a voltage gain of 15 and a power budget of 3 mW. Assume $R_G \approx 10(r_{O1} || r_{O2})$ and the dc level of the output must be equal to $V_{DD}/2$.

- 7.65.** The CS stage of Fig. 7.87 incorporates a degenerated PMOS current source. The degeneration must raise the output impedance of the current source to about $10r_{O1}$ such that the voltage gain remains nearly equal to the intrinsic gain of M_1 . Assume $\lambda = 0.1 \text{ V}^{-1}$ for both transistors and a power budget of 2 mW.

- (a) If $V_B = 1 \text{ V}$, determine the values of $(W/L)_2$ and R_S so that the impedance seen looking into the drain of M_2 is equal to $10r_{O1}$.
 (b) Determine $(W/L)_1$ to achieve a voltage gain of 30.

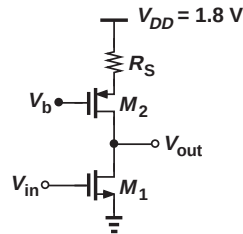


Figure 7.87

- 7.66.** Assuming a power budget of 1 mW and an overdrive of 200 mV for M_1 , design the circuit shown in Fig. 7.88 for a voltage gain of 4.

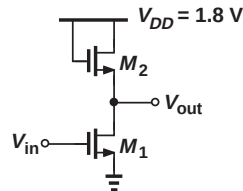


Figure 7.88

- 7.67.** Design the common-gate stage depicted in Fig. 7.89 for an input impedance of 50 Ω and a voltage gain of 5. Assume a power budget of 3 mW.

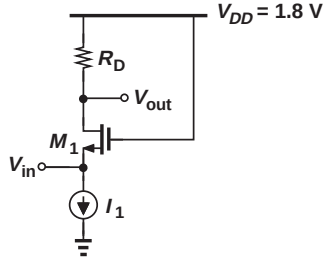


Figure 7.89

- 7.68.** Design the circuit of Fig. 7.90 such that M_1 operates 100 mV away from the triode region while providing a voltage gain of 4. Assume a power budget of 2 mW.

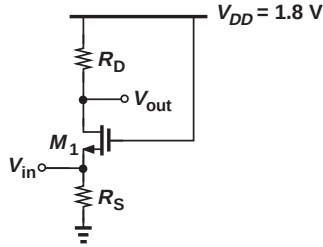


Figure 7.90

- 7.69.** Figure 7.91 shows a self-biased common-gate stage, where $R_G \approx 10R_D$ and C_G serves as a low impedance so that the voltage gain is still given by $g_m R_D$. Design the circuit for a power budget of 5 mW and a voltage gain of 5. Assume $R_S \approx 10/g_m$ so that the input impedance remains approximately equal to $1/g_m$.

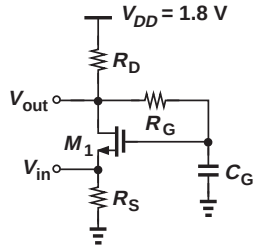


Figure 7.91

- 7.70.** Design the CG stage shown in Fig. 7.92 such that it can accommodate an output swing of 500 mV_{pp}, i.e., V_{out} can fall below its bias value by 250 mV without driving

M_1 into the triode region. Assume a voltage gain of 4 and an input impedance of 50 Ω . Select $R_S \approx 10/g_m$ and $R_1 + R_2 = 20$ k Ω . (Hint: since M_1 is biased 250 mV away from the triode region, we have $R_S I_D + V_{GS} - V_{TH} + 250$ mV = $V_{DD} - I_D R_D$.)

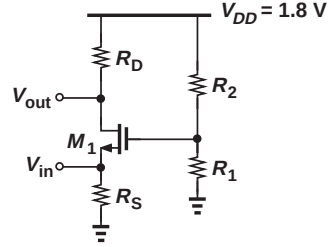


Figure 7.92

- 7.71.** Design the source follower depicted in Fig. 7.93 for a voltage gain of 0.8 and a power budget of 2 mW. Assume the output dc level is equal to $V_{DD}/2$ and the input impedance exceeds 10 k Ω .

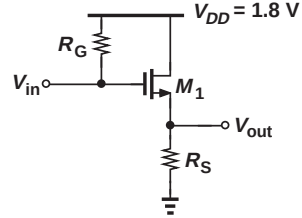


Figure 7.93

- 7.72.** Consider the source follower shown in Fig. 7.94. The circuit must provide a voltage gain of 0.6 at 100 MHz. Design the circuit such that the dc voltage at node X is equal to $V_{DD}/2$. Assume the input impedance exceeds 20 k Ω .

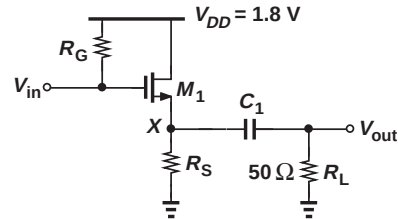


Figure 7.94

7.73. In the source follower of Fig. 7.95, M_2 serves as a current source. The circuit must operate with a power budget of 3 mW, a voltage gain of 0.9, and a minimum allowable output of 0.3 V (i.e., M_2 must remain in saturation if $V_{DS2} \geq 0.3$ V). Assuming $\lambda = 0.1 \text{ V}^{-1}$ for both transistors, design the circuit.

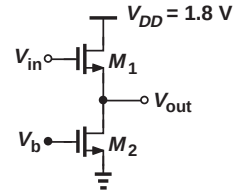


Figure 7.95

SPICE PROBLEMS

In the following problems, use the MOS models and source/drain dimensions given in Appendix A. Assume the substrates of NMOS and PMOS devices are tied to ground and V_{DD} , respectively.

7.74. In the circuit of Fig. 7.96, I_1 is an ideal current source equal to 1 mA.

- Using hand calculations, determine $(W/L)_1$ such that $g_{m1} = (100 \Omega)^{-1}$.
- Select C_1 for an impedance of $\approx 100 \Omega$ ($\ll 1 \text{ k}\Omega$) at 50 MHz.
- Simulate the circuit and obtain the voltage gain and output impedance at 50 MHz.
- What is the change in the gain if I_1 varies by $\pm 20\%$?

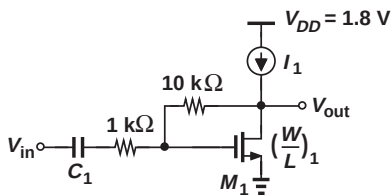


Figure 7.96

7.75. The source follower of Fig. 7.97 employs a bias current source, M_2 .

- What value of V_{in} places M_2 at the edge of saturation?
- What value of V_{in} places M_1 at the edge of saturation?
- Determine the voltage gain if V_{in} has a dc value of 1.5 V.

- What is the change in the gain if V_b changes by $\pm 50 \text{ mV}$?

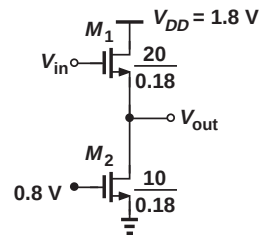


Figure 7.97

7.76. Figure 7.98 depicts a cascade of a source follower and a common-gate stage. Assume $V_b = 1.2 \text{ V}$ and $(W/L)_1 = (W/L)_2 = 10 \mu\text{m}/0.18 \mu\text{m}$.

- Determine the voltage gain if V_{in} has a dc value of 1.2 V.
- Verify that the gain drops if the dc value of V_{in} is higher or lower than 1.2 V.
- What dc value at the input reduces the gain by 10% with respect to that obtained in (a)?

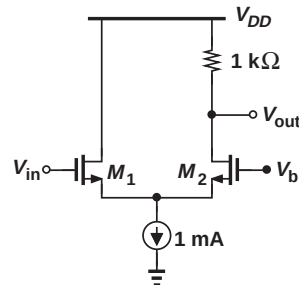


Figure 7.98

7.77. Consider the CS stage shown in Fig. 7.99, where M_2 operates as a resistor.

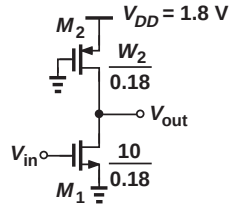


Figure 7.99

- Determine W_2 such that an input dc level of 0.8 V yields an output dc level of 1 V. What is the voltage gain under these conditions?
- What is the change in the gain if the mobility of the NMOS device varies by

$\pm 10\%$? Can you explain this result using the expressions derived in Chapter 6 for the transconductance?

7.78. Repeat Problem 7.77 for the circuit illustrated in Fig. 7.100 and compare the sensitivities to the mobility.

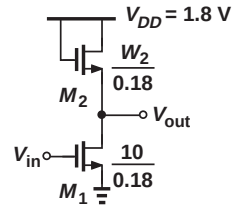


Figure 7.100