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The Islamic University of Gaza

Computer Architecture Lab - 2023

LAB (3) || Memory Design

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objective

1. What is a memory, and how it behavior from working module?
2. Design memory units and understand how it operates during read and write operation.
3. Designing Memory for given parameter.

Memory

Memory is basically a device that has the capacity to store information. A memory unit is the amount of data that the memory can hold. Besides, we measure this storage capacity in terms of bytes. Moreover, there are different units of memory as per the requirement.

Primary Memory

This is the internal memory that stores the data and instructions of the CPU. It is volatile in nature (data is lost when the power is disconnected).

The primary memory has two types:

1. RAM (Random Access Memory)
As per the name, data can be accessed randomly and quickly.
2. ROM (Read Only Memory)
As per the name, we can only read data and cannot write (store) to it.

Units of Memory

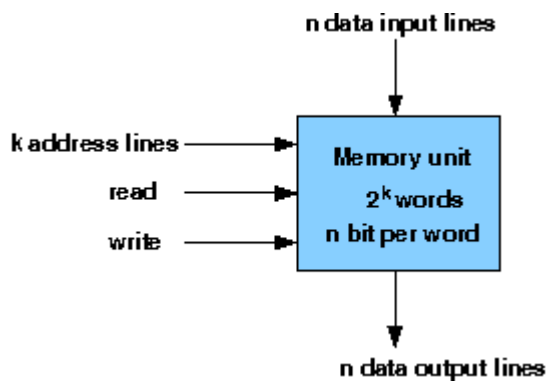
The storage capacity of the memory is expressed in various units of memory. These are as follows:

- **Bit, Byte, Word, Kilobyte, Megabyte, Gigabyte, Terabyte**

A computer word is similar to a byte, as it is also a group of bits

Design of Memory

A memory unit is a collection of storage cells together with associated circuits needed to transform information in and out of the device. Memory cells which can be accessed for information transfer to or from any desired random location is called random access memory(RAM). The block diagram of a memory unit-



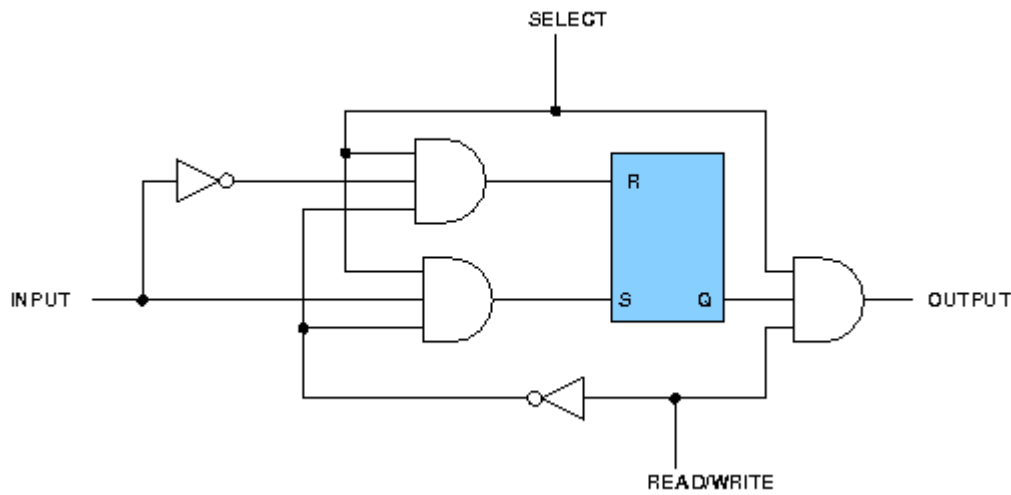
The n data input lines provide the information to be stored in memory, and the n data output lines supply the information coming out of particular word chosen among the 2^k available inside the memory.

The **internal construction** of a random-access memory of **m words** with **n bits per word** consists of **$m \times n$ binary storage cells** and associated decoding circuits for selecting individual words.

The binary cell is the basic building block of a memory unit.

Design of a RAM cell

The logic diagram is: 3 AND Gate, 2 Not Gate and Set-Reset (SR) flip flop.



The binary cell has three inputs and one output as:

- The select input enables the cell for reading or writing.
- The read/write input determines the cell operation when it is selected.

A **1** in the read/write input provides the **read** operation by forming a path from the flip-flop to the output terminal.

A **0** in the read/write input provides the **write** operation by forming a path from the input terminal to the flip-flop.

Task(1):

- simulate the logic diagram of RAM cell and give truth table

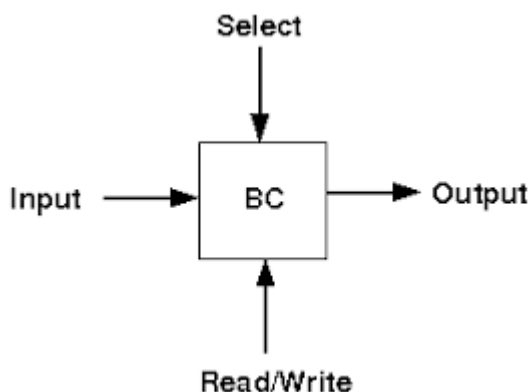
Design of a 4X4 RAM :

The logical construction of a small RAM 4X4 is shown below.

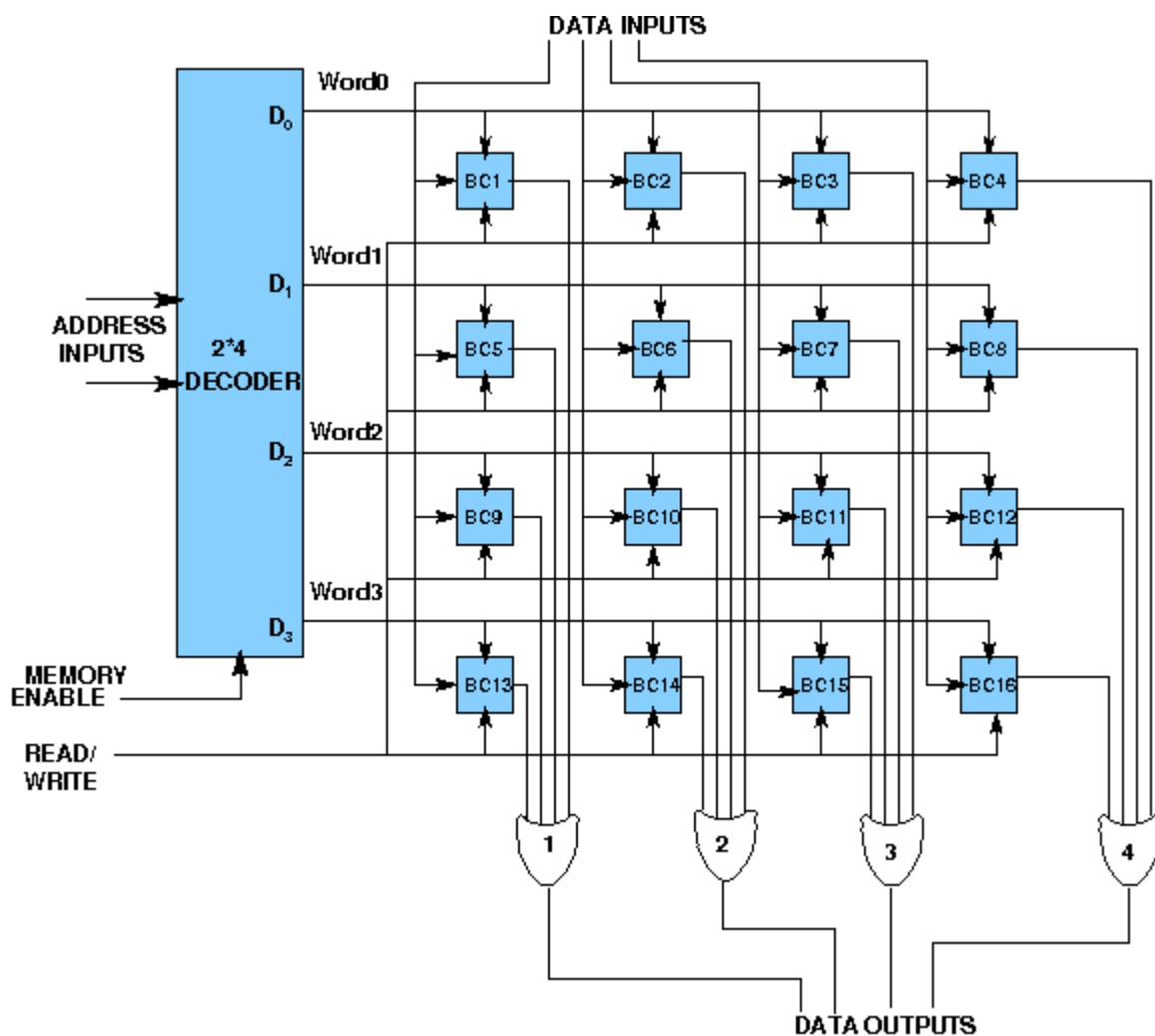
It consists of 4 words of 4 bits each and has a total of 16 binary cells.

Each block labeled BC represents the binary cell with its 3 inputs and 1 output.

Block Diagram



- A memory with 4 words needs two address lines.
- The two address inputs go through a 2^4 decoder to select one of the four words. The decoder is enabled with the memory enable input.
- When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected.
- With the memory enable at 1, one of the four words is selected, dictated by the value in the two address lines. Once a word has been selected, the read/write input determines the operation.
- During the read operation the four bits of the selected word go through OR gates to the output terminals.
- During the write operation, the data available in the input lines transferred into the four binary cells of the selected word.



try :

1. Do some read operation by properly setting the R/W', memory enable then give input and check the output.
2. Do some write operation by properly setting the R/W', memory enable then give input and check the output.
3. Do some read operation without setting the memory enable but properly setting the R/W' then give input and check the output

Assignment Statements:

Ex1:

Design a 4X3 RAM memory which will have 4 words each of 3 bits using binary RAM cells, decoder with enable, OR gates and test it by giving proper input.